Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8180, 2.50 GHz)

**SPECrate®2017_fp_base = 257**
**SPECrate®2017_fp_peak = 258**

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name</td>
<td>Intel Xeon Platinum 8180</td>
</tr>
<tr>
<td>Max MHz</td>
<td>3800</td>
</tr>
<tr>
<td>Nominal</td>
<td>2500</td>
</tr>
<tr>
<td>Enabled</td>
<td>56 cores, 2 chips, 2 threads/core</td>
</tr>
<tr>
<td>Orderable</td>
<td>1.2 Chips</td>
</tr>
<tr>
<td>Cache L1</td>
<td>32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>Cache L2</td>
<td>1 MB I+D on chip per core</td>
</tr>
<tr>
<td>Cache L3</td>
<td>38.5 MB I+D on chip per core</td>
</tr>
<tr>
<td>Other Memory</td>
<td>None</td>
</tr>
<tr>
<td>Memory</td>
<td>384 GB (24 x 16 GB 2Rx4 PC4-2666V-R)</td>
</tr>
<tr>
<td>Storage</td>
<td>1 x 1 TB SAS HDD, 10K RPM</td>
</tr>
<tr>
<td>Other</td>
<td>None</td>
</tr>
</tbody>
</table>

**Software**

- **OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.103-92.56-default
- **Compiler:** C/C++: Version 18.0.2.199 of Intel C/C++ Compiler for Linux;
  Fortran: Version 18.0.2.199 of Intel Fortran Compiler for Linux
- **Parallel:** No
- **Firmware:** Version 3.2.3c released Mar-2018
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** None
- **Power Management:** --
# SPEC CPU®2017 Floating Point Rate Result

## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8180, 2.50 GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base = 257</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_peak = 258</td>
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</table>

### CPU2017 License:
9019

### Test Sponsor:
Cisco Systems

### Tested by:
Cisco Systems

### Test Date:
May-2018

### Hardware Availability:
Aug-2017

### Software Availability:
Mar-2018

## Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>112</td>
<td>2326</td>
<td>483</td>
<td>2326</td>
<td>483</td>
<td>2326</td>
<td>483</td>
<td>112</td>
<td>2326</td>
<td>483</td>
<td>2325</td>
<td>483</td>
<td>2326</td>
<td>483</td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>112</td>
<td>572</td>
<td>248</td>
<td>574</td>
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<td>573</td>
<td>247</td>
<td>112</td>
<td>575</td>
<td>247</td>
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<td>247</td>
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<td>246</td>
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<tr>
<td>508.namd_r</td>
<td>112</td>
<td>451</td>
<td>236</td>
<td>450</td>
<td>236</td>
<td>452</td>
<td>235</td>
<td>112</td>
<td>447</td>
<td>238</td>
<td>448</td>
<td>237</td>
<td>446</td>
<td>238</td>
</tr>
<tr>
<td>510.parest_r</td>
<td>112</td>
<td>2434</td>
<td>120</td>
<td>2440</td>
<td>120</td>
<td>2440</td>
<td>120</td>
<td>112</td>
<td>2464</td>
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<td>2464</td>
<td>119</td>
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<tr>
<td>511.povray_r</td>
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<td>707</td>
<td>370</td>
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<td>370</td>
<td>712</td>
<td>368</td>
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<td>441</td>
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<td>519.lbm_r</td>
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<td>120</td>
</tr>
<tr>
<td>521.wrf_r</td>
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<td>217</td>
<td>1155</td>
<td>217</td>
<td>112</td>
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<td>218</td>
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<td>217</td>
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<td>526.blender_r</td>
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<td>341</td>
<td>112</td>
<td>495</td>
<td>344</td>
<td>497</td>
<td>343</td>
<td>495</td>
<td>345</td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>112</td>
<td>667</td>
<td>294</td>
<td>670</td>
<td>293</td>
<td>670</td>
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<td>112</td>
<td>662</td>
<td>296</td>
<td>663</td>
<td>295</td>
<td>662</td>
<td>296</td>
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<td>538.imagick_r</td>
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<td>364</td>
<td>764</td>
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<td>763</td>
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<td>112</td>
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<td>762</td>
<td>365</td>
<td>764</td>
<td>365</td>
<td>764</td>
</tr>
<tr>
<td>544.nab_r</td>
<td>112</td>
<td>332</td>
<td>567</td>
<td>333</td>
<td>566</td>
<td>331</td>
<td>570</td>
<td>112</td>
<td>388</td>
<td>486</td>
<td>391</td>
<td>482</td>
<td>391</td>
<td>482</td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>112</td>
<td>2752</td>
<td>159</td>
<td>2755</td>
<td>158</td>
<td>2759</td>
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<td>112</td>
<td>2755</td>
<td>158</td>
<td>2758</td>
<td>158</td>
<td>2752</td>
<td>159</td>
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<tr>
<td>554.roms_r</td>
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<td>1878</td>
<td>94.8</td>
<td>1886</td>
<td>94.8</td>
<td>1876</td>
<td>94.9</td>
<td>112</td>
<td>1871</td>
<td>95.1</td>
<td>1863</td>
<td>95.5</td>
<td>1871</td>
<td>95.1</td>
</tr>
</tbody>
</table>

## Submit Notes

The taskset mechanism was used to bind copies to processors. The config file option 'submit' was used to generate taskset commands to bind each copy to a specific processor.

For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## General Notes

Environment variables set by runcpu before the start of the run:

```bash
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"
```

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.4

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3>       /proc/sys/vm/drop_caches
```

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8180, 2.50 GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECraté®2017_fp_base = 257
SPECraté®2017_fp_peak = 258

Test Date: May-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

General Notes (Continued)
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-uezu Wed May 16 01:31:53 2018

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

- model name : Intel(R) Xeon(R) Platinum 8180 CPU @ 2.50GHz
- 2 "physical id"s (chips)
- 112 "processors"
- cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  - cpu cores : 28
  - siblings : 56
  - physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30
  - physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30

From lscpu:
- Architecture: x86_64
- CPU op-mode(s): 32-bit, 64-bit
- Byte Order: Little Endian
- CPU(s):
- On-line CPU(s) list: 0-111
- Thread(s) per core: 2
- Core(s) per socket: 28
- Socket(s):
- NUMA node(s): 4
- Vendor ID: GenuineIntel
- CPU family: 6

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8180, 2.50 GHz)

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Test Date:</td>
<td>May-2018</td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Aug-2017</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Mar-2018</td>
</tr>
</tbody>
</table>

**SPEC CPU®2017 Floating Point Rate Result**

**SPECrates**
- **SPECrate®2017_fp_base** = 257
- **SPECrate®2017_fp_peak** = 258

### Platform Notes (Continued)

- **Model:** 85
- **Model name:** Intel(R) Xeon(R) Platinum 8180 CPU @ 2.50GHz
- **Stepping:** 4
- **CPU MHz:** 1018.638
- **CPU max MHz:** 3800.0000
- **CPU min MHz:** 1000.0000
- **BogoMIPS:** 4999.98
- **Virtualization:** VT-x
- **L1d cache:** 32K
- **L1i cache:** 32K
- **L2 cache:** 1024K
- **L3 cache:** 39424K
- **NUMA node0 CPU(s):** 0-3, 7-9, 14-17, 21-23, 56-59, 63-65, 70-73, 77-79
- **NUMA node1 CPU(s):** 4-6, 10-13, 18-20, 24-27, 60-62, 66-69, 74-76, 80-83
- **NUMA node2 CPU(s):** 28-31, 35-37, 42-45, 49-51, 84-87, 91-93, 98-101, 105-107
- **NUMA node3 CPU(s):** 32-34, 38-41, 46-48, 52-55, 88-90, 94-97, 102-104, 108-111
- **Flags:** fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc aperfmpreperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpre pdcm pclid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts dtherm hwlp hwlp_act_window hwp_epp hwp_pkg_req intel_pt spec_ctrl kaiser tpr_shadow vsnmi flexpriority ept vpid fsgsbase tsc_adjust bml1 hle avx2 smep bmi2 erts invpudid rtm cqm mpx avx512f avx512dq rdseed advx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_1lc cqm_occup_llc

From `numactl --hardware`

**Warning:** a numactl 'node' might or might not correspond to a physical chip.

<table>
<thead>
<tr>
<th>Available:</th>
<th>4 nodes (0-3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Node 0 cpus:</td>
<td>0 1 2 3 7 8 9 14 15 16 17 21 22 23 56 57 58 59 63 64 65 70 71 72 73 77 78 79</td>
</tr>
<tr>
<td>Node 0 size:</td>
<td>95320 MB</td>
</tr>
<tr>
<td>Node 0 free:</td>
<td>95092 MB</td>
</tr>
<tr>
<td>Node 1 cpus:</td>
<td>4 5 6 10 11 12 13 18 19 20 24 25 26 27 60 61 62 66 67 68 69 74 75 76 80 81 82 83</td>
</tr>
<tr>
<td>Node 1 size:</td>
<td>96753 MB</td>
</tr>
<tr>
<td>Node 1 free:</td>
<td>96518 MB</td>
</tr>
<tr>
<td>Node 2 cpus:</td>
<td>28 29 30 31 35 36 37 42 43 44 45 49 50 51 84 85 86 87 91 92 93 98 99 100 101 105 106 107</td>
</tr>
<tr>
<td>Node 2 size:</td>
<td>96753 MB</td>
</tr>
<tr>
<td>Node 2 free:</td>
<td>96516 MB</td>
</tr>
<tr>
<td>Node 3 cpus:</td>
<td>32 33 34 38 39 40 41 46 47 48 52 53 54 55 58 88 89 90 94 95 96 97 102 103 104 108 109 110 111</td>
</tr>
</tbody>
</table>

(Continued on next page)
Platform Notes (Continued)

node 0 1 2 3
0: 10 11 21 21
1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10

From /proc/meminfo
MemTotal: 394831632 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
SuSE-release:
  SUSE Linux Enterprise Server 12 (x86_64)
  VERSION = 12
  PATCHLEVEL = 2
  # This file is deprecated and will be removed in a future service pack or release.
  # Please check /etc/os-release for details about this release.
os-release:
  NAME="SLES"
  VERSION="12-SP2"
  VERSION_ID="12.2"
  PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
  ID="sles"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
Linux linux-uezu 4.4.103-92.56-default #1 SMP Wed Dec 27 16:24:31 UTC 2017 (2fd2155)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jan 2 03:00

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 xfs 894G 450G 445G 51% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
  BIOS Cisco Systems, Inc. B200M5.3.2.3c.0.0307181316 03/07/2018
  Memory:
  24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8180, 2.50 GHz)

SPECrate®2017_fp_base = 257
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: May-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Platform Notes (Continued)

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C                | 519.libm_r(base, peak) 538.imagick_r(base, peak)
| 544.nab_r(base, peak)
==============================================================================
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
==============================================================================

C++              | 508.namd_r(base, peak) 510.parest_r(base, peak)
==============================================================================
icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
==============================================================================

C++, C            | 511.povray_r(base, peak) 526.blender_r(base, peak)
==============================================================================
icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
==============================================================================

C++, C, Fortran  | 507.cactuBSSN_r(base, peak)
==============================================================================
icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
==============================================================================

Fortran          | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
| 554.roms_r(base, peak)
==============================================================================
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

(Continued on next page)
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Compiler Version Notes (Continued)

-----------------------------------------------------------------------------
Fortran, C      | 521.wrf_r(base, peak) 527.cam4_r(base, peak)
-----------------------------------------------------------------------------
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
-----------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64

(Continued on next page)
Cisco Systems
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Base Portability Flags (Continued)

544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

C++ benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

Fortran benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

Benchmarks using Fortran, C, and C++:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

(Continued on next page)
Cisco Systems  
Cisco UCS B200 M5 (Intel Xeon Platinum 8180, 2.50 GHz)  

SPECrate®2017_fp_base = 257  
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CPU2017 License:  9019  
Test Sponsor:  Cisco Systems  
Test Date:  May-2018  
Tested by:  Cisco Systems  
Hardware Availability:  Aug-2017  
Software Availability:  Mar-2018  

Peak Compiler Invocation (Continued)

Benchmarks using both Fortran and C:  
 ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:  
 icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:  
 icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
519.lbm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3

538.imagick_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3

544.nab_r: Same as 519.lbm_r

C++ benchmarks:
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3

Fortran benchmarks:
503.bwaves_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte

549.fotonik3d_r: Same as 503.bwaves_r

554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -nostandard-realloc-lhs

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8180, 2.50 GHz)

SPECrate®2017_fp_base = 257
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Peak Optimization Flags (Continued)

554.roms_r (continued):
-align array32byte

Benchmarks using both Fortran and C:
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

Benchmarks using Fortran, C, and C++:
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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