**NEC Corporation**

Express5800/D120h (Intel Xeon Gold 6152)

<table>
<thead>
<tr>
<th>SPECspeed2017_fp_base</th>
<th>SPECspeed2017_fp_peak</th>
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<tr>
<td>112</td>
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**CPU2017 License**: 9006  
**Test Date**: Jun-2018  
**Test Sponsor**: NEC Corporation  
**Hardware Availability**: Jan-2018  
**Tested by**: NEC Corporation  
**Software Availability**: Mar-2018

**Threads**

- **603.bwaves_s**: 44 threads (Specspeed2017_fp_base: 150, Specspeed2017_fp_peak: 469)
- **607.cactuBSSN_s**: 44 threads (Specspeed2017_fp_base: 752, Specspeed2017_fp_peak: 42.3)
- **619.lbm_s**: 44 threads (Specspeed2017_fp_base: 42.3, Specspeed2017_fp_peak: 150)
- **621.wrf_s**: 44 threads (Specspeed2017_fp_base: 80.9, Specspeed2017_fp_peak: 42.3)
- **627.cam4_s**: 44 threads (Specspeed2017_fp_base: 42.3, Specspeed2017_fp_peak: 150)
- **628.pop2_s**: 44 threads (Specspeed2017_fp_base: 61.5, Specspeed2017_fp_peak: 80.9)
- **638.imagick_s**: 44 threads (Specspeed2017_fp_base: 61.5, Specspeed2017_fp_peak: 80.9)
- **644.nab_s**: 44 threads (Specspeed2017_fp_base: 61.5, Specspeed2017_fp_peak: 80.9)
- **649.fotonik3d_s**: 44 threads (Specspeed2017_fp_base: 61.5, Specspeed2017_fp_peak: 80.9)
- **654.roms_s**: 44 threads (Specspeed2017_fp_base: 61.5, Specspeed2017_fp_peak: 80.9)

**Hardware**

- **CPU Name**: Intel Xeon Gold 6152  
- **Max MHz.**: 3700  
- **Nominal**: 2100  
- **Enabled**: 44 cores, 2 chips  
- **Orderable**: 1,2 chips  
- **L1 Cache**: 32 KB I + 32 KB D on chip per core  
- **L2 Cache**: 1 MB I+D on chip per core  
- **L3 Cache**: 30.25 MB I+D on chip per core  
- **Memory**: 384 GB (12 x 32 GB 2Rx4 PC4-2666V-R)  
- **Storage**: 1 x 1 TB SATA, 7200 RPM  
- **Other**: None

**Software**

- **OS**: Red Hat Enterprise Linux Server release 7.4 (Maipo)  
- **Kernel**: 3.10.0-693.21.1.el7.x86_64  
- **Compiler**: C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux; Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux  
- **Parallel**: Yes  
- **Firmware**: Version F21 02/22/2018 released Apr-2018  
- **File System**: ext4  
- **System State**: Run level 3 (multi-user)  
- **Base Pointers**: 64-bit  
- **Peak Pointers**: 64-bit  
- **Other**: None
SPEC CPU2017 Floating Point Speed Result

NEC Corporation

Express5800/D120h (Intel Xeon Gold 6152)

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SPECspeed2017_fp_base = 112
SPECspeed2017_fp_peak = 114

Results Table

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</tr>
</tbody>
</table>

SPECspeed2017_fp_base = 112
SPECspeed2017_fp_peak = 114

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3 > /proc/sys/vm/drop_caches

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
**SPEC CPU2017 Floating Point Speed Result**

NEC Corporation

Express5800/D120h (Intel Xeon Gold 6152)

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CPU2017 License: 9006  
Test Sponsor: NEC Corporation  
Tested by: NEC Corporation  
Test Date: Jun-2018  
Hardware Availability: Jan-2018  
Software Availability: Mar-2018

**Platform Notes**

BIOS Settings:
- ENERGY_PERF_BIAS_CFG mode: Performance
- Hyper-Threading [ALL]: Disable
- LLC dead line alloc: Disable
- Patrol Scrub: Disable
- DCU Streamer Prefetch: Disable
- Adjacent Cache Prefetch: Disable
- Sysinfo program /home/cpu2017/bin/sysinfo
- Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
- running on d120h Wed Jun 6 02:53:48 2018

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
- model name: Intel(R) Xeon(R) Gold 6152 CPU @ 2.10GHz
- 2 "physical id"s (chips)
- 44 "processors"
- cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  - cpu cores: 22
  - siblings: 22
  - physical 0: cores 0 1 2 3 4 5 8 9 10 11 12 16 17 18 19 20 21 24 25 26 27 28
  - physical 1: cores 0 1 2 3 4 5 8 9 10 11 12 16 17 18 19 20 21 24 25 26 27 28

From lscpu:
- Architecture: x86_64
- CPU op-mode(s): 32-bit, 64-bit
- Byte Order: Little Endian
- CPU(s): 44
- On-line CPU(s) list: 0-43
- Thread(s) per core: 1
- Core(s) per socket: 22
- Socket(s): 2
- NUMA node(s): 2
- Vendor ID: GenuineIntel
- CPU family: 6
- Model: 85
- Model name: Intel(R) Xeon(R) Gold 6152 CPU @ 2.10GHz
- Stepping: 4
- CPU MHz: 3196.429
- CPU max MHz: 3700.0000
- CPU min MHz: 1000.0000
- BogoMIPS: 4200.00
- Virtualization: VT-x
- L1d cache: 32K

(Continued on next page)
SPEC CPU2017 Floating Point Speed Result

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SPECspeed2017_fp_base = 112
SPECspeed2017_fp_peak = 114

Platform Notes (Continued)

L1i cache: 32K
L2 cache: 1024K
L3 cache: 30976K
NUMA node0 CPU(s): 0-21
NUMA node1 CPU(s): 22-43
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pebs bts rep_good ncpu osf1 xtopology nonstop_tsc
aperfmperf eagerfpu nni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 fma
cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch epb cat_l3 cdp_l3 invpcid_single
intel_pt spec_ctrl ibpb_support tpr_shadow vmmi flexpriority ept vpid fsgsbase
tsc_adjust bmi1 hle avx2 smep bmi2 iberms invpcid rtm cqm mpx rdt_a avx512f avx512dq
rdsseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsaves opt xgetbv1
cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local dtherm ida arat pln pts hwp
hwp_act_window hwp_epp hwp_pkg_req

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.

node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21
node 0 size: 195236 MB
node 0 free: 190317 MB
node 1 cpus: 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43
node 1 size: 196608 MB
node 1 free: 191913 MB
node distances:

From /proc/meminfo
MemTotal: 394644400 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /proc/meminfo

(Continued on next page)
COMPILER VERSION NOTES

---

CC 619.lbm_s(base) 638.imagick_s(base, peak) 644.nab_s(base, peak)
---

icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
---

---

CC 619.lbm_s(peak)
---

icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
---

---

FC 607.cactuBSSN_s(base)

(Continued on next page)
NEC Corporation

Express5800/D120h (Intel Xeon Gold 6152)

SPEC CPU2017 Floating Point Speed Result

SPECspeed2017_fp_base = 112
SPECspeed2017_fp_peak = 114

CPU2017 License: 9006
Test Sponsor: NEC Corporation
Test Date: Jun-2018
Tested by: NEC Corporation
Hardware Availability: Jan-2018
Software Availability: Mar-2018

Compiler Version Notes (Continued)

icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
FC  607.cactuBSSN_s(peak)
------------------------------------------------------------------------------
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
FC  603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)
------------------------------------------------------------------------------
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
FC  603.bwaves_s(peak) 649.fotonik3d_s(peak) 654.roms_s(peak)
------------------------------------------------------------------------------
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
CC  621.wrf_s(base) 627.cam4_s(base, peak) 628.pop2_s(base)
------------------------------------------------------------------------------
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
CC  621.wrf_s(peak) 628.pop2_s(peak)
------------------------------------------------------------------------------
ifort (IFORT) 18.0.0 20170811

(Continued on next page)
NEC Corporation
Express5800/D120h (Intel Xeon Gold 6152)

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CPU2017 License: 9006
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**Compiler Version Notes (Continued)**

Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

**Base Compiler Invocation**

C benchmarks:
icc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

**Base Portability Flags**

603.bwaves.s: -DSPEC_LP64
607.cactuBSSN.s: -DSPEC_LP64
619.lbm.s: -DSPEC_LP64
621.wrf.s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4.s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2.s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
   -assume byterecl
638.imagick.s: -DSPEC_LP64
644.nab.s: -DSPEC_LP64
649.fotonik3d.s: -DSPEC_LP64
654.roms.s: -DSPEC_LP64

**Base Optimization Flags**

C benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch

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NEC Corporation

Express5800/D120h (Intel Xeon Gold 6152)

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CPU2017 License: 9006
Test Sponsor: NEC Corporation
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Test Date: Jun-2018
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Base Optimization Flags (Continued)

Fortran benchmarks (continued):
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte

Benchmarks using Fortran, C, and C++:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte

Base Other Flags

C benchmarks:
-m64 -std=c11

Fortran benchmarks:
-m64

Benchmarks using both Fortran and C:
-m64 -std=c11

Benchmarks using Fortran, C, and C++:
-m64 -std=c11

Peak Compiler Invocation

C benchmarks:
icc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort
SPEC CPU2017 Floating Point Speed Result

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Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

619.lbm_s: basepeak = yes

638.imagick_s: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP

644.nab_s: Same as 638.imagick_s

Fortran benchmarks:

603.bwaves_s: basepeak = yes

649.fotonik3d_s: basepeak = yes

654.roms_s: -prof-gen(pass 1) -prof-use(pass 2) -DSPEC_SUPPRESS_OPENMP -DSPEC_OPENMP -O2 -xCORE-AVX2 -qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div -qopt-mem-layout-trans=3 -qopenmp -nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:

621.wrf_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX2 -qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div -qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte

627.cam4_s: basepeak = yes

628.pop2_s: Same as 621.wrf_s

Benchmarks using Fortran, C, and C++:

-prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX2 -qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div -qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte
SPEC CPU2017 Floating Point Speed Result

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Express5800/D120h (Intel Xeon Gold 6152)

| SPECspeed2017_fp_base = 112 |
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CPU2017 License: 9006
Test Sponsor: NEC Corporation
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Test Date: Jun-2018
Hardware Availability: Jan-2018
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Peak Other Flags

C benchmarks:
- m64 -std=c11

Fortran benchmarks:
- m64

Benchmarks using both Fortran and C:
- m64 -std=c11

Benchmarks using Fortran, C, and C++:
- m64 -std=c11

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/NEC-Platform-Settings-V1.2-D120h-RevA.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/NEC-Platform-Settings-V1.2-D120h-RevA.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU2017 v1.0.2 on 2018-06-05 13:53:47-0400.