Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6148 2.40 GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
CPU Name: Intel Xeon Gold 6148
Max MHz.: 3700
Nominal: 2400
Enabled: 40 cores, 2 chips
Orderable: 1,2 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 27.5 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2666V-R)
Storage: 1 x 240 GB M.2 SATA SSD
Other: None

OS: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.120-92.70-default
Compiler: C/C++: Version 19.0.1.144 of Intel C/C++ Compiler for Linux;
Fortran: Version 19.0.1.144 of Intel Fortran Compiler for Linux
Parallel: Yes
Firmware: Version 4.0.1 released Oct-2018
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 32/64-bit
Other: jemalloc memory allocator V5.0.1

SPEC® CPU2017 Integer Speed Result
Copyright 2017-2019 Standard Performance Evaluation Corporation

SPECspeed2017_int_base = 9.09
SPECspeed2017_int_peak = 9.37

Threads

600.perlbench_s 40
602gcc_s 40
605mcf_s 40
620omnetpp_s 40
623xalancbmk_s 40
625x264_s 40
631deepsjeng_s 40
641leela_s 40
648exchange2_s 40
657xz_s 40

--- SPECspeed2017_int_base (9.09) ---
--- SPECspeed2017_int_peak (9.37) ---

Hardware

Software
### SPEC CPU2017 Integer Speed Result

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SPECspeed2017_int_base = 9.09  
SPECspeed2017_int_peak = 9.37

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>40</td>
<td>285</td>
<td>6.24</td>
<td>281</td>
<td>6.31</td>
<td>281</td>
<td>6.33</td>
<td>236</td>
<td>7.51</td>
<td>237</td>
<td>7.48</td>
<td></td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>40</td>
<td>430</td>
<td>11.0</td>
<td>425</td>
<td>11.1</td>
<td>427</td>
<td>11.1</td>
<td>427</td>
<td>11.1</td>
<td>426</td>
<td>11.1</td>
<td></td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>40</td>
<td>239</td>
<td>6.82</td>
<td>232</td>
<td>7.03</td>
<td>254</td>
<td>6.41</td>
<td>232</td>
<td>7.03</td>
<td>231</td>
<td>7.05</td>
<td></td>
</tr>
<tr>
<td>623.xalanchmk_s</td>
<td>40</td>
<td>148</td>
<td>9.54</td>
<td>150</td>
<td>9.48</td>
<td>149</td>
<td>9.51</td>
<td>139</td>
<td>10.2</td>
<td>138</td>
<td>10.2</td>
<td></td>
</tr>
<tr>
<td>625.x264_s</td>
<td>40</td>
<td>135</td>
<td>13.1</td>
<td>135</td>
<td>13.1</td>
<td>135</td>
<td>13.1</td>
<td>135</td>
<td>13.1</td>
<td>135</td>
<td>13.1</td>
<td></td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>40</td>
<td>277</td>
<td>5.17</td>
<td>277</td>
<td>5.17</td>
<td>278</td>
<td>5.16</td>
<td>280</td>
<td>5.12</td>
<td>280</td>
<td>5.12</td>
<td></td>
</tr>
<tr>
<td>641.leela_s</td>
<td>40</td>
<td>377</td>
<td>4.52</td>
<td>377</td>
<td>4.53</td>
<td>377</td>
<td>4.53</td>
<td>378</td>
<td>4.52</td>
<td>378</td>
<td>4.51</td>
<td></td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>40</td>
<td>220</td>
<td>13.4</td>
<td>219</td>
<td>13.4</td>
<td>219</td>
<td>13.5</td>
<td>219</td>
<td>13.3</td>
<td>219</td>
<td>13.5</td>
<td></td>
</tr>
<tr>
<td>657.xz_s</td>
<td>40</td>
<td>279</td>
<td>22.2</td>
<td>279</td>
<td>22.2</td>
<td>279</td>
<td>22.1</td>
<td>275</td>
<td>22.4</td>
<td>276</td>
<td>22.4</td>
<td></td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

#### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

#### General Notes

Environment variables set by runcpu before the start of the run:

KMP_AFFINITY = "granularity=fine,scatter"

LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"

OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.4

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3 > /proc/sys/vm/drop_caches
```

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

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SPECspeed2017_int_base = 9.09
SPECspeed2017_int_peak = 9.37

Test Date: Jan-2019
Hardware Availability: Aug-2017
Software Availability: Nov-2018

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bce8f2999c33d61f64985e45859ea9
running on linux-x58q Sat Jan 19 10:05:55 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6148 CPU @ 2.40GHz
  2 "physical id"s (chips)
  40 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 20
siblings : 20
physical 0: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
physical 1: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 40
On-line CPU(s) list: 0-39
Thread(s) per core: 1
Core(s) per socket: 20
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6148 CPU @ 2.40GHz
Stepping: 4
CPU MHz: 3003.729
CPU max MHz: 3700.0000
CPU min MHz: 1000.0000
BogoMIPS: 4788.72
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K

(Continued on next page)
Platform Notes (Continued)

L2 cache: 1024K
L3 cache: 28160K
NUMA node0 CPU(s): 0-19
NUMA node1 CPU(s): 20-39
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmperf eagerfpu nni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pfn pts
dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt rsb_ctxsw spec_ctrl stibp
retropoline kaiser tpr_shadow vmvi flexpriority ept vpid fsgsbase tsc_adjust bm1 hle
avx2 smep bmi2 ems invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt
c1wb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
  node 0 size: 385626 MB
  node 0 free: 385067 MB
  node 1 cpus: 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39
  node 1 size: 387054 MB
  node 1 free: 386684 MB
  node distances:
    node 0 1
    0: 10 21
    1: 21 10

From /proc/meminfo
  MemTotal: 791225144 kB
  HugePages_Total: 0
  Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
  SuSE-release:
    SUSE Linux Enterprise Server 12 (x86_64)
    VERSION = 12
    PATCHLEVEL = 2
    # This file is deprecated and will be removed in a future service pack or release.
    # Please check /etc/os-release for details about this release.
    os-release:
      NAME="SLES"
      VERSION="12-SP2"

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Version: 12.2
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
Linux linux-x58q 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Mitigation: PTI
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: IBRS+IBPB

run-level 3 Jan 19 00:01

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 xfs 210G 28G 183G 13% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.4.0.1.139.1003182220 10/03/2018
Memory:
24x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
CC  600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base) 625.x264_s(base, peak) 657.xz_s(base)
------------------------------------------------------------------------------
icc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
==============================================================================

==============================================================================
CC  600.perlbench_s(peak) 602.gcc_s(peak) 605.mcf_s(peak) 657.xz_s(peak)
------------------------------------------------------------------------------
icc (ICC) 19.0.1.144 20181018

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**Compiler Version Notes (Continued)**

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

```
CXXC 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)
   641.leela_s(base)
icpc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

CXXC 620.omnetpp_s(peak) 623.xalancbmk_s(peak) 631.deepsjeng_s(peak)
   641.leela_s(peak)
icpc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

FC 648.exchange2_s(base, peak)
ifort (IFORT) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
```

**Base Compiler Invocation**

C benchmarks:
- `icc -m64 -std=c11`

C++ benchmarks:
- `icpc -m64`

Fortran benchmarks:
- `ifort -m64`

**Base Portability Flags**

- `600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64`
- `602.gcc_s: -DSPEC_LP64`
- `605.mcf_s: -DSPEC_LP64`
- `620.omnetpp_s: -DSPEC_LP64`

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Hardware Availability: Aug-2017
Software Availability: Nov-2018

Base Portability Flags (Continued)

623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leea_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks (except as noted below):
icpc -m64

623.xalancbmk_s: icpc -m32 -L/opt/intel/lib/ia32

Fortran benchmarks:
ifort -m64

Peak Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64

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Peak Portability Flags (Continued)

602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:

600.perlbench_s: -Wl, -z, multiprocess -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=3 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -fno-strict-overflow
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

602.gcc_s: -Wl, -z, multiprocess -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=3 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -L/home/cpu2017/je5.0.1-64/ -ljemalloc

605.mcf_s: -Wl, -z, multiprocess -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

625.x264_s: -Wl, -z, multiprocess -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

657.xz_s: Same as 602.gcc_s

C++ benchmarks:

620.omnetpp_s: -Wl, -z, multiprocess -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

(Continued on next page)
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Peak Optimization Flags (Continued)

623.xalanbmk_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-L/home/cpu2017/je5.0.1-32/ -ljemalloc

631.deepsjeng_s: Same as 620.omnetpp_s

641.leela_s: Same as 620.omnetpp_s

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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