**SPEC CPU®2017 Integer Speed Result**

**Hewlett Packard Enterprise**
(Test Sponsor: HPE)
ProLiant DL560 Gen10  
(2.70 GHz, Intel Xeon Platinum 8280)

<table>
<thead>
<tr>
<th>SPECspeed®2017_int_base</th>
<th>SPECspeed®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>10.3</td>
<td>Not Run</td>
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</tbody>
</table>

CPU2017 License: 3  
Test Sponsor: HPE  
Tested by: HPE

Test Date: Mar-2019  
Hardware Availability: Apr-2019  
Software Availability: Feb-2019

<table>
<thead>
<tr>
<th>Threads</th>
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<tr>
<td>600.perbench_s</td>
<td>28</td>
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<tr>
<td>602.gcc_s</td>
<td>28</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>28</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>28</td>
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<tr>
<td>623.xalancbmk_s</td>
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<tr>
<td>625.x264_s</td>
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<tr>
<td>631.deepsjeng_s</td>
<td>28</td>
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<tr>
<td>641.leela_s</td>
<td>28</td>
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<tr>
<td>648.exchange2_s</td>
<td>28</td>
</tr>
<tr>
<td>657.xz_s</td>
<td>28</td>
</tr>
</tbody>
</table>

**Hardware**

- CPU Name: Intel Xeon Platinum 8280
- Max MHz: 4000
- Nominal: 2700
- Enabled: 28 cores, 1 chip
- Orderable: 1, 2, 4 chip(s)
- Cache L1: 32 KB I + 32 KB D on chip per core
- L2: 1 MB I+D on chip per core
- L3: 38.5 MB I+D on chip per chip
- Other: None
- Memory: 192 GB (6 x 32 GB 2Rx4 PC4-2933Y-R)
- Storage: 1 x 400 GB SATA SSD, RAID 0
- Other: None

**Software**

- OS: SUSE Linux Enterprise Server 15 (x86_64)  
  Kernel 4.12.14-23-default
- Compiler: C++: Version 19.0.2.187 of Intel C/C++  
  Compiler Build 20190117 for Linux;  
  Fortran: Version 19.0.2.187 of Intel Fortran  
  Compiler Build 20190117 for Linux
- Parallel: Yes
- Firmware: HPE BIOS Version U34 02/02/2019 released Apr-2019
- File System: btrfs
- System State: Run level 3 (multi-user)
- Base Pointers: 64-bit
- Peak Pointers: Not Applicable
- Other: jemalloc memory allocator V5.0.1
- Power Management: --
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Results Table

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<thead>
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</tbody>
</table>

SPECspeed®2017_int_base = 10.3
SPECspeed®2017_int_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
  sync; echo 3 > /proc/sys/vm/drop_caches

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017_u2/lib/ia32:/home/cpu2017_u2/lib/intel64"
LD_LIBRARY_PATH = "$LD_LIBRARY_PATH:/home/cpu2017_u2/je5.0.1-32:/home/cpu2017_u2/je5.0.1-64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
Hewlett Packard Enterprise  
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CPU2017 License: 3
Test Sponsor: HPE
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Test Date: Mar-2019
Hardware Availability: Apr-2019
Software Availability: Feb-2019

Platform Notes

BIOS Configuration:
Hyper-Threading set to Disabled
Thermal Configuration set to Maximum Cooling
Memory Patrol Scrubbing set to Disabled
LLC Prefetch set to Enabled
LLC Dead Line Allocation set to Disabled
Enhanced Processor Performance set to Enabled
Workload Profile set to General Peak Frequency Compute
Energy/Performance Bias set to Maximum Performance
Workload Profile set to Custom
Uncore Frequency Scaling set to Auto
Numa Group Size Optimization set to Flat
Advanced Memory Protection set to AdvancedECC

Sysinfo program /home/cpu2017_u2/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-vqdi Mon Mar 11 23:06:29 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Platinum 8280 CPU @ 2.70GHz
   1 "physical id"s (chips)
   28 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 28
siblings : 28
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 28
On-line CPU(s) list: 0-27
Thread(s) per core: 1
Core(s) per socket: 28
Socket(s): 1
NUMA node(s): 1
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Platinum 8280 CPU @ 2.70GHz
Stepping: 7

(Continued on next page)
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Platform Notes (Continued)

CPU MHz: 2700.000
BogoMIPS: 5400.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 39424K
NUMA node0 CPU(s): 0-27
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acp mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 cdp_l3 invpcid_single intel_ppin mba tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erts invpcid rtm cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 xsavec qm_llc qm_occuc_llc qm_mbmb_total qm_mbmb_local ibpb ibrs dtherm ida arat pin pts pkup ospke avx512_vnni arch_capabilities ssbd

/proc/cpuinfo cache data
cache size : 39424 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 1 nodes (0)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27
node 0 size: 193086 MB
node 0 free: 192404 MB
node distances:
node 0
0: 10

From /proc/meminfo
MemTotal: 197720576 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"

(Continued on next page)
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Platform Notes (Continued)

cpe://o:suse:sles:15

uname -a:
Linux linux-vqdi 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBBP, IBRS_FW

run-level 3 Mar 11 23:05

SPEC is set to: /home/cpu2017_u2

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS HPE U34 02/02/2019
Memory:
42x UNKNOWN NOT AVAILABLE
6x UNKNOWN NOT AVAILABLE 32 GB 2 rank 2933

Compiler Version Notes

==============================================================================
C       | 600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base)
| 625.x264_s(base) 657.xz_s(base)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.2.187 Build 20190117
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

C++     | 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)
| 641.leela_s(base)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
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Compiler Version Notes (Continued)

Version 19.0.2.187 Build 20190117
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-W1, -z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

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Base Optimization Flags (Continued)

C benchmarks (continued):
-`L=/home/cpu2017_u2/je5.0.1-64/ -ljemalloc`

C++ benchmarks:
-`-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
-`-qopt-mem-layout-trans=4`
-`-L=/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64`
-`-lqkmalloc`

Fortran benchmarks:
-`-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4`
-`-nostandard-realloc-lhs`

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/HPE-ic19.0u1-flags-linux64.html
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revA.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/HPE-ic19.0u1-flags-linux64.xml
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revA.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.