Lenovo Global Technology
ThinkSystem SD530
(2.80 GHz, Intel Xeon Gold 6242)

CPU2017 License: 9017
Test Sponsor: Lenovo Global Technology
Tested by: Lenovo Global Technology

Test Date: May-2019
Hardware Availability: Apr-2019
Software Availability: Nov-2018

SPECrate2017_int_base = 212
SPECrate2017_int_peak = Not Run

500.perlbench_r 64
502.gcc_r 64
505.mcf_r 64
520.omnetpp_r 64
523.xalancbmk_r 64
525.x264_r 64
531.deepsjeng_r 64
541.leela_r 64
548.exchange2_r 64
557.xz_r 64

Copies

Hardware
CPU Name: Intel Xeon Gold 6242
Max MHz.: 3900
Nominal: 2800
Enabled: 32 cores, 2 chips, 2 threads/core
Orderable: 1.2 chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 22 MB I+D on chip per chip
Other: None
Memory: 384 GB (12 x 32 GB 2Rx4 PC4-2933Y-R)
Storage: 1 x 800 GB SATA SSD
Other: None

Software
OS: SUSE Linux Enterprise Server 15 (x86_64)
Compiler: C/C++: Version 19.0.1.144 of Intel C/C++
Compiler Build 20181018 for Linux:
Fortran: Version 19.0.1.144 of Intel Fortran
Compiler Build 20181018 for Linux
Parallel: No
Firmware: Lenovo BIOS Version TEE135R 2.10 released Feb-2019
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: None
## Results Table

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</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## General Notes

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH = "/home/cpu2017-1.0.5-ic19.0u1/lib/intel64"
```

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3 > /proc/sys/vm/drop_caches
```

runcpu command invoked through numactl i.e.: numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
General Notes (Continued)

is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2018-3640 (Spectre variant 3a) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2018-3639 (Spectre variant 4) is mitigated in the system as tested and documented.

Platform Notes

BIOS configuration:
Choose Operating Mode set to Maximum Performance
Choose Operating Mode set to Custom Mode
DCU Streamer Prefetcher set to Disable
MONITOR/MWAIT set to Enable
SNC set to Enable
Sysinfo program /home/cpu2017-1.0.5-ic19.0u1/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-qxkw Mon May 27 15:20:06 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Gold 6242 CPU @ 2.80GHz
  2 "physical id"s (chips)
  64 "processors"
  cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 16
  siblings : 32
  physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
  physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu:

Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 64
On-line CPU(s) list: 0-63
Thread(s) per core: 2
Core(s) per socket: 16
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85

(Continued on next page)
### SPEC CPU2017 Integer Rate Result

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**SPECrate2017_int_base** = 212  
**SPECrate2017_int_peak** = Not Run

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**Platform Notes (Continued)**

- **Model name:** Intel(R) Xeon(R) Gold 6242 CPU @ 2.80GHz
- **Stepping:** 6
- **CPU MHz:** 2800.000
- **CPU max MHz:** 3900.0000
- **CPU min MHz:** 1200.0000
- **BogoMIPS:** 5600.00
- **Virtualization:** VT-x
- **L1d cache:** 32K
- **L1i cache:** 32K
- **L2 cache:** 1024K
- **L3 cache:** 22528K
- **NUMA node0 CPU(s):** 0-3,8-11,32-35,40-43
- **NUMA node1 CPU(s):** 4-7,12-15,36-39,44-47
- **NUMA node2 CPU(s):** 16-19,24-27,48-51,56-59
- **NUMA node3 CPU(s):** 20-23,28-31,52-55,60-63

---

**Flags:**

- fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
- pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtsscp
- lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
- aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
- xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
- avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3
- invpcid_single ssbd mba ibrs ibpb tpr_shadow vmmi flexpriority ept vpid
- fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ets m*)) invpcid rdtscp cpl rdtc
- arch_capabilities

---

From `numactl --hardware`

```
WARNING: a numactl 'node' might or might not correspond to a physical chip.
```

```
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 8 9 10 11 32 33 34 35 40 41 42 43
node 0 size: 96367 MB
node 0 free: 92811 MB
node 1 cpus: 4 5 6 7 12 13 14 15 36 37 38 39 44 45 46 47
node 1 size: 96754 MB
node 1 free: 96338 MB
node 2 cpus: 16 17 18 19 24 25 26 27 48 49 50 51 56 57 58 59
node 2 size: 96754 MB
node 2 free: 96181 MB
node 3 cpus: 20 21 22 23 28 29 30 31 52 53 54 55 60 61 62 63
node 3 size: 96723 MB
node 3 free: 96296 MB
node distances:
  node 0 1 2 3
```

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SPEC CPU2017 Integer Rate Result
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SPECrate2017_int_base = 212
SPECrate2017_int_peak = Not Run

Platform Notes (Continued)
(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
CC  500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base) 525.x264_r(base)
   557.xz_r(base)
-----------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
   Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
-----------------------------------------------------------------------------

==============================================================================
CXXC 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base)
   541.leela_r(base)
-----------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
   Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
-----------------------------------------------------------------------------

==============================================================================
FC  548.exchange2_r(base)
-----------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
   64, Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
-----------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64
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### Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64  
502.gcc_r: -DSPEC_LP64  
505.mcf_r: -DSPEC_LP64  
520.omnetpp_r: -DSPEC_LP64  
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX  
525.x264_r: -DSPEC_LP64  
531.deepsjeng_r: -DSPEC_LP64  
541.keela_r: -DSPEC_LP64  
548.exchange2_r: -DSPEC_LP64  
557.xz_r: -DSPEC_LP64

### Base Optimization Flags

**C benchmarks:**  
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64  
-lqkmalloc

**C++ benchmarks:**  
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64  
-lqkmalloc

**Fortran benchmarks:**  
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64  
-lqkmalloc

The flags files that were used to format this result can be browsed at  
http://www.spec.org/cpu2017/flags/Lenovo-Platform-SPECcpu2017-Flags-V1.2-CLX-A.html

You can also download the XML flags sources by saving the following links:  
http://www.spec.org/cpu2017/flags/Lenovo-Platform-SPECcpu2017-Flags-V1.2-CLX-A.xml
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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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