### Dell Inc. PowerEdge M640 (Intel Xeon Silver 4214, 2.20GHz)

| CPU2017 License: | 55 |
| Test Sponsor: | Dell Inc. |
| Tested by: | Dell Inc. |
| Test Date: | Mar-2019 |
| Hardware Availability: | Apr-2019 |
| Software Availability: | Feb-2019 |

#### SPEC CPU2017 Integer Speed Result

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<td>gcc_s</td>
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<td>mcf_s</td>
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<td>x264_s</td>
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<td>deepsjeng_s</td>
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<td>leela_s</td>
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<tr>
<td>xz_s</td>
<td>16.9</td>
<td>17.0</td>
</tr>
</tbody>
</table>

### Hardware

- **CPU Name:** Intel Xeon Silver 4214
- **Max MHz.:** 3200
- **Nominal:** 2200
- **Enabled:** 24 cores, 2 chips
- **Orderable:** 1.2 chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 16.5 MB I+D on chip per chip
- **Other:** None
- **Memory:** 384 GB (12 x 32 GB 2Rx4 PC4-2933Y-R, running at 2400)
- **Storage:** 1 x 480 GB SATA SSD
- **Other:** None

### Software

- **OS:** Ubuntu 18.04.2 LTS
- **Compiler:** C/C++: Version 19.0.1.144 of Intel C/C++ Compiler Build 20181018 for Linux;
  Fortran: Version 19.0.1.144 of Intel Fortran Compiler Build 20181018 for Linux
- **Parallel:** Yes
- **Firmware:** Version 2.3.1 released May-2019
- **File System:** ext4
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** jemalloc memory allocator V5.0.1
SPEC CPU2017 Integer Speed Result

Dell Inc.

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SPECspeed2017_int_base = 8.00
SPECspeed2017_int_peak = 8.17

Results Table

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SPECspeed2017_int_base = 8.00
SPECspeed2017_int_peak = 8.17

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
  sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

(Continued on next page)
Dell Inc.  
PowerEdge M640 (Intel Xeon Silver 4214, 2.20GHz)  

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**General Notes (Continued)**

jemalloc, a general purpose malloc implementation  
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5  

**Platform Notes**

BIOS settings:  
ADDDC setting disabled  
Sub NUMA Cluster enabled  
Virtualization Technology disabled  
DCU Streamer Prefetcher enabled  
System Profile set to Custom  
CPU Performance set to Maximum Performance  
C States set to Autonomous  
C1E disabled  
Uncore Frequency set to Dynamic  
Energy Efficiency Policy set to Performance  
Memory Patrol Scrub disabled  
Logical Processor disabled  
CPU Interconnect Bus Link Power Management disabled  
PCI ASPM L1 Link Power Management disabled  
Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9  
running on intel-sut Fri May 10 17:15:29 2019

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see  
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

model name: Intel(R) Xeon(R) Silver 4214 CPU @ 2.20GHz  
2 "physical id"s (chips)  
24 "processors"  
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)  
cpu cores: 12  
siblings: 12  
physical 0: cores 0 1 2 3 4 5 8 9 10 11 12 13  
physical 1: cores 0 1 2 3 4 5 8 9 10 11 12 13

From lscpu:  
Architecture: x86_64  
CPU op-mode(s): 32-bit, 64-bit  
Byte Order: Little Endian  
CPU(s): 24  
On-line CPU(s) list: 0-23

(Continued on next page)
SPEC CPU2017 Integer Speed Result

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CPU2017 License: 55
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Software Availability: Feb-2019

Platform Notes (Continued)

Thread(s) per core: 1
Core(s) per socket: 12
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4214 CPU @ 2.20GHz
Stepping: 6
CPU MHz: 2948.942
BogoMIPS: 4400.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 16896K
NUMA node0 CPU(s): 0,2,4,6,8,10,12,14,16,18,20,22
NUMA node1 CPU(s): 1,3,5,7,9,11,13,15,17,19,21,23
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt retpcp aes xsave avx f16c rdrand
lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_pni
ssbd mba ibrs ibpb ibrs_enhanced tpr_shadow vmxset flexpriority ept vpid
fsal fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erts invpcid rtm cqm mpx rdtsa_a avx512f
avx512dq rdseed rdQed adx smap cflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsavesopt xsaveopt xsave xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mqm_total cqm_mqm_local
dtherm ida arat pfn pku opkpe avx512_vnni flush_l1d arch_capabilities

Warning: the node might not correspond to a physical chip.

From numactl --hardware

Available: 2 nodes (0-1)
node 0 cpus: 0 2 4 6 8 10 12 14 16 18 20 22
node 0 size: 191914 MB
node 0 free: 191584 MB
node 1 cpus: 1 3 5 7 9 11 13 15 17 19 21 23
node 1 size: 193512 MB
node 1 free: 192979 MB
node distances:
node 0 1
0: 10 21
1: 21 10

(Continued on next page)
SPEC CPU2017 Integer Speed Result

Dell Inc. PowerEdge M640 (Intel Xeon Silver 4214, 2.20GHz)

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**SPECspeed2017_int_base = 8.00**  
**SPECspeed2017_int_peak = 8.17**

### Platform Notes (Continued)

From /proc/meminfo
- MemTotal: 394676604 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

/usr/bin/lsb_release -d
- Ubuntu 18.04.2 LTS

From /etc/*release* /etc/*version*
- debain_version: buster/sid
- os-release:
  - NAME="Ubuntu"
  - VERSION="18.04.2 LTS (Bionic Beaver)"
  - ID=ubuntu
  - ID_LIKE=debian
  - PRETTY_NAME="Ubuntu 18.04.2 LTS"
  - VERSION_ID="18.04"
  - HOME_URL="https://www.ubuntu.com/"
  - SUPPORT_URL="https://help.ubuntu.com/"

uname -a:
- Linux intel-sut 4.15.0-45-generic #48-Ubuntu SMP Tue Jan 29 16:28:13 UTC 2019 x86_64
- x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
- CVE-2017-5754 (Meltdown): Not affected
- CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
- CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB

run-level 3 May 10 17:07

SPEC is set to: /home/cpu2017
- Filesystem Type Size Used Avail Use% Mounted on
  - /dev/sda2 ext4 439G 19G 398G 5% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

- BIOS Dell Inc. 2.3.1 05/02/2019
- Memory:
  - 6x 00AD00B300AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933, configured at 2400
  - 6x 00AD069D00AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933, configured at 2400
  - 4x Not Specified Not Specified

(End of data from sysinfo program)
## Dell Inc. 
PowerEdge M640 (Intel Xeon Silver 4214, 2.20GHz)

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### Compiler Version Notes

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<th>Compiler</th>
<th>Base Invocation</th>
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</table>
| CC        | 600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base) 625.x264_s(base, peak) 657.xz_s(base)
| Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.1.144 Build 20181018
| Copyright (C) 1985-2018 Intel Corporation. All rights reserved.                                                                                                                                                                                                                                                                                                                                                       |
| CC        | 600.perlbench_s(peak) 602.gcc_s(peak) 605.mcf_s(peak) 657.xz_s(peak)
| Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.1.144 Build 20181018
| Copyright (C) 1985-2018 Intel Corporation. All rights reserved.                                                                                                                                                                                                                                                                                                                                                       |
| CXXC      | 620.omnetpp_s(base) 623.xalancbmk_s(base, peak) 631.deepsjeng_s(base, peak) 641.leela_s(base, peak)
| Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.1.144 Build 20181018
| Copyright (C) 1985-2018 Intel Corporation. All rights reserved.                                                                                                                                                                                                                                                                                                                                                       |
| CXXC      | 620.omnetpp_s(peak)
| Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.1.144 Build 20181018
| Copyright (C) 1985-2018 Intel Corporation. All rights reserved.                                                                                                                                                                                                                                                                                                                                                       |
| FC        | 648.exchange2_s(base, peak)
| Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.1.144 Build 20181018
| Copyright (C) 1985-2018 Intel Corporation. All rights reserved.                                                                                                                                                                                                                                                                                                                                                       |

### Base Compiler Invocation

- C benchmarks:
- `icc -m64 -std=c11`
**SPEC CPU2017 Integer Speed Result**

**Dell Inc.**

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### Base Compiler Invocation (Continued)

- **C++ benchmarks:**
  - icpc -m64

- **Fortran benchmarks:**
  - ifort -m64

---

### Base Portability Flags

- 600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
- 602.gcc_s: -DSPEC_LP64
- 605.mcf_s: -DSPEC_LP64
- 620.omnetpp_s: -DSPEC_LP64
- 623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
- 625.x264_s: -DSPEC_LP64
- 631.deepsjeng_s: -DSPEC_LP64
- 641.leela_s: -DSPEC_LP64
- 648.exchange2_s: -DSPEC_LP64
- 657.xz_s: -DSPEC_LP64

---

### Base Optimization Flags

- **C benchmarks:**
  - -W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
  - -qopt-mem-layout-trans=4 -gopenmp -DSPEC_OPENMP
  - -L/usr/local/je5.0.1-64/lib -ljemalloc

- **C++ benchmarks:**
  - -W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
  - -qopt-mem-layout-trans=4
  - -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64
  - -lqkmalloc

- **Fortran benchmarks:**
  - -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4
  - -nostandard-realloc-lhs
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Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2  
-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3  
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp  
-DSPEC_OPENMP -fno-strict-overflow  
-L/usr/local/je5.0.1-64/lib -ljemalloc

602.gcc_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2  
-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3  
-no-prec-div -DSPEC_SUPPRESS_OPENMP  
-L/usr/local/je5.0.1-64/lib -ljemalloc

605.mcf_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4  
-DSPEC_SUPPRESS_OPENMP -gopenmp -DSPEC_OPENMP  
-L/usr/local/je5.0.1-64/lib -ljemalloc

625.x264_s: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4 -gopenmp -DSPEC_OPENMP  
-L/usr/local/je5.0.1-64/lib -ljemalloc

657.xz_s: -Wl,-z,muldefs -xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3  
-no-prec-div -DSPEC_SUPPRESS_OPENMP -gopenmp  
-DSPEC_OPENMP -L/usr/local/je5.0.1-64/lib -ljemalloc

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## SPEC CPU2017 Integer Speed Result

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### CPU2017 License:
55

**Test Sponsor:** Dell Inc.

**Hardware Availability:** Apr-2019

**Tested by:** Dell Inc.

**Software Availability:** Feb-2019

### Peak Optimization Flags (Continued)

**C++ benchmarks:**

620.omnetpp_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-DSPEC_SUPPRESS_OPENMP
-1/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64
-lqkmalloc

623.xalancbmk_s: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-1/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64
-lqkmalloc

631.deepsjeng_s: Same as 623.xalancbmk_s

641.leela_s: Same as 623.xalancbmk_s

**Fortran benchmarks:**

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs

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The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:


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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

**Tested with SPEC CPU2017 v1.0.5 on 2019-05-10 13:15:28-0400.**


Originally published on 2019-06-25.