Hewlett Packard Enterprise
(Test Sponsor: HPE)
Synergy 480 Gen10
(2.60 GHz, Intel Xeon Gold 6240M)

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Threads 600.perbench_s 36
          602.gcc_s 36
          605.mcf_s 36
          620.omnetpp_s 36
          623.xalancbmk_s 36
          625.x264_s 36
          631.deepsjeng_s 36
          641.leela_s 36
          648.exchange2_s 36
          657.xz_s 36

SPECspeed2017_int_base = 9.85
SPECspeed2017_int_peak = Not Run

Hardware
CPU Name: Intel Xeon Gold 6240M
Max MHz.: 3900
Nominal: 2600
Enabled: 36 cores, 2 chips
Orderable: 1, 2 chip(s)
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 24.75 MB I+D on chip per chip
Other: None
Memory: 384 GB (24 x 16 GB 2Rx8 PC4-2933Y-R)
Storage: 1 x 400 GB SAS SSD, RAID 0
Other: None

Software
OS: SUSE Linux Enterprise Server 15 (x86_64)
Compiler: C/C++: Version 19.0.2.187 of Intel C/C++
Compiler Build 20190117 for Linux;
Fortran: Version 19.0.2.187 of Intel Fortran
Compiler Build 20190117 for Linux
Parallel: Yes
Firmware: HPE BIOS Version I42 02/02/2019 released Apr-2019
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: jemalloc memory allocator V5.0.1
SPEC CPU2017 Integer Speed Result

Hewlett Packard Enterprise
(Test Sponsor: HPE)
Synergy 480 Gen10
(2.60 GHz, Intel Xeon Gold 6240M)

SPECspeed2017_int_base = 9.85
SPECspeed2017_int_peak = Not Run

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Test Date: May-2019
Hardware Availability: Apr-2019
Software Availability: Feb-2019

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>36</td>
<td>262</td>
<td>6.78</td>
<td>260</td>
<td>6.82</td>
<td>261</td>
<td>6.81</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>36</td>
<td><strong>428</strong></td>
<td><strong>9.31</strong></td>
<td>427</td>
<td>9.33</td>
<td>428</td>
<td>9.30</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>36</td>
<td>378</td>
<td>12.5</td>
<td>380</td>
<td>12.4</td>
<td><strong>379</strong></td>
<td><strong>12.5</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>36</td>
<td>208</td>
<td>7.83</td>
<td>206</td>
<td>7.92</td>
<td><strong>206</strong></td>
<td><strong>7.90</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>623.xalancbmk_s</td>
<td>36</td>
<td>115</td>
<td>12.3</td>
<td><strong>116</strong></td>
<td><strong>12.2</strong></td>
<td>118</td>
<td>12.0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>625.x264_s</td>
<td>36</td>
<td>125</td>
<td>14.1</td>
<td><strong>125</strong></td>
<td><strong>14.1</strong></td>
<td>125</td>
<td>14.1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>36</td>
<td><strong>264</strong></td>
<td><strong>5.43</strong></td>
<td>264</td>
<td>5.43</td>
<td>263</td>
<td>5.44</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>641.leela_s</td>
<td>36</td>
<td>360</td>
<td>4.74</td>
<td><strong>360</strong></td>
<td><strong>4.75</strong></td>
<td>359</td>
<td>4.75</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>36</td>
<td><strong>211</strong></td>
<td><strong>13.9</strong></td>
<td>211</td>
<td>13.9</td>
<td>210</td>
<td>14.0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>657.xz_s</td>
<td>36</td>
<td><strong>278</strong></td>
<td><strong>22.2</strong></td>
<td>278</td>
<td>22.2</td>
<td>278</td>
<td>22.3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

SPECspeed2017_int_base = 9.85
SPECspeed2017_int_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3 > /proc/sys/vm/drop_caches

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017_u2/lib/ia32:/home/cpu2017_u2/lib/intel64:
/home/cpu2017_u2/je5.0.1-32:/home/cpu2017_u2/je5.0.1-64"
OMP_STACKSIZE = "192M"
Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3 > /proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

(Continued on next page)
Hewlett Packard Enterprise
(Test Sponsor: HPE)
Synergy 480 Gen10
(2.60 GHz, Intel Xeon Gold 6240M)

SPECspeed2017_int_base = 9.85
SPECspeed2017_int_peak = Not Run

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Test Date: May-2019
Hardware Availability: Apr-2019
Software Availability: Feb-2019

General Notes (Continued)


Platform Notes

BIOS Configuration:
Hyper-Threading set to Disabled
Thermal Configuration set to Maximum Cooling
Memory Patrol Scrubbing set to Disabled
LLC Prefetch set to Enabled
LLC Dead Line Allocation set to Disabled
Enhanced Processor Performance set to Enabled
Workload Profile set to General Peak Frequency Compute
Minimum Processor Idle Power Core C-State set to C0E State
Energy/Performance Bias set to Balanced Power
Workload Profile set to Custom
Numa Group Size Optimization set to Flat
Sysinfo program /home/cpu2017_u2/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on sy480g10-2 Fri May 31 13:15:40 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6240M CPU @ 2.60GHz
  2  "physical id"s (chips)
  36 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 18
siblings : 18
  physical 0: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
  physical 1: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 36
On-line CPU(s) list: 0-35
Thread(s) per core: 1
Core(s) per socket: 18
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel

(Continued on next page)
## SPEC CPU2017 Integer Speed Result

---

### Hewlett Packard Enterprise

(Prueba realizada por: HPE)

**Synergy 480 Gen10**

(2.60 GHz, Intel Xeon Gold 6240M)

---

**SPECspeed2017_int_base = 9.85**

**SPECspeed2017_int_peak = Not Run**

---

### Platform Notes (Continued)

<table>
<thead>
<tr>
<th>CPU family:</th>
<th>6</th>
</tr>
</thead>
<tbody>
<tr>
<td>Model:</td>
<td>85</td>
</tr>
<tr>
<td>Model name:</td>
<td>Intel(R) Xeon(R) Gold 6240M CPU @ 2.60GHz</td>
</tr>
<tr>
<td>Stepping:</td>
<td>7</td>
</tr>
<tr>
<td>CPU MHz:</td>
<td>2600.000</td>
</tr>
<tr>
<td>BogoMIPS:</td>
<td>5200.00</td>
</tr>
<tr>
<td>Virtualization:</td>
<td>VT-x</td>
</tr>
<tr>
<td>L1d cache:</td>
<td>32K</td>
</tr>
<tr>
<td>L1i cache:</td>
<td>32K</td>
</tr>
<tr>
<td>L2 cache:</td>
<td>1024K</td>
</tr>
<tr>
<td>L3 cache:</td>
<td>25344K</td>
</tr>
<tr>
<td>NUMA node0 CPU(s):</td>
<td>0-17</td>
</tr>
<tr>
<td>NUMA node1 CPU(s):</td>
<td>18-35</td>
</tr>
<tr>
<td>Flags:</td>
<td>fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault ebт cat_l3 cdp_l3 invpcid_single intel_ppin mba tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ersed invpcid rtm cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local ibpb ibrs stibp dtlb dtherm ida arat pln pts pku ospke avx512_vnni arch_capabilities ssbd</td>
</tr>
</tbody>
</table>

/proclist/cpuninfo cache data

```plaintext
cache size : 25344 KB
```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```plaintext
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
node 0 size: 193017 MB
node 0 free: 192392 MB
node 1 cpus: 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35
node 1 size: 193334 MB
node 1 free: 193148 MB
node distances:
node 0 1
0: 10 21
1: 21 10
```

From /proc/meminfo

```plaintext
MemTotal: 395624792 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
```

(Continued on next page)
Hewlett Packard Enterprise
(Test Sponsor: HPE)
Synergy 480 Gen10
(2.60 GHz, Intel Xeon Gold 6240M)

<table>
<thead>
<tr>
<th>SPECspeed2017_int_base</th>
<th>9.85</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed2017_int_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Test Date: May-2019
Hardware Availability: Apr-2019
Software Availability: Feb-2019

Compiler Version Notes

(Continued on next page)
# SPEC CPU2017 Integer Speed Result

**Hewlett Packard Enterprise**  
(Test Sponsor: HPE)  
Synergy 480 Gen10  
(2.60 GHz, Intel Xeon Gold 6240M)  

<table>
<thead>
<tr>
<th>SPECspeed2017_int_base</th>
<th>9.85</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed2017_int_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>HPE</td>
</tr>
<tr>
<td>Tested by:</td>
<td>HPE</td>
</tr>
</tbody>
</table>

**Compiler Version Notes (Continued)**

Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---

CXXC 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)  
641.leela_s(base)

---

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.2.187 Build 20190117  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---

FC 648.exchange2_s(base)

---

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.0.2.187 Build 20190117  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---

## Base Compiler Invocation

**C benchmarks:**

```bash
icc -m64 -std=c11
```

**C++ benchmarks:**

```bash
icpc -m64
```

**Fortran benchmarks:**

```bash
ifort -m64
```

## Base Portability Flags

```
600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64
```
### SPEC CPU2017 Integer Speed Result

**Hewlett Packard Enterprise**
(Test Sponsor: HPE)
Synergy 480 Gen10
(2.60 GHz, Intel Xeon Gold 6240M)

<table>
<thead>
<tr>
<th>SPECspeed2017_int_base</th>
<th>9.85</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed2017_int_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 3  
**Test Sponsor:** HPE  
**Tested by:** HPE

#### Base Optimization Flags

**C benchmarks:**
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP  
-L/home/cpu2017_u2/je5.0.1-64/ -ljemalloc

**C++ benchmarks:**
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64  
-lqkmalloc

**Fortran benchmarks:**
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4  
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at:

- [http://www.spec.org/cpu2017/flags/HPE-ic19.0u1-flags-linux64.html](http://www.spec.org/cpu2017/flags/HPE-ic19.0u1-flags-linux64.html)
- [http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.html](http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.html)

You can also download the XML flags sources by saving the following links:

- [http://www.spec.org/cpu2017/flags/HPE-ic19.0u1-flags-linux64.xml](http://www.spec.org/cpu2017/flags/HPE-ic19.0u1-flags-linux64.xml)
- [http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.xml](http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.xml)

---

SPEC is a registered trademark of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU2017 v1.0.5 on 2019-05-31 14:15:39-0400.