### Hardware

<table>
<thead>
<tr>
<th>Software</th>
<th>OS:</th>
<th>SUSE Linux Enterprise Server 15 (x86_64)</th>
</tr>
</thead>
<tbody>
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<td>Compiler:</td>
<td>C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux</td>
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</tr>
<tr>
<td>Parallel:</td>
<td>No</td>
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<tr>
<td>Firmware:</td>
<td>Version 4.0.4c released Apr-2019</td>
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<tr>
<td>File System:</td>
<td>xfs</td>
<td></td>
</tr>
<tr>
<td>System State:</td>
<td>Run level 3 (multi-user)</td>
<td></td>
</tr>
<tr>
<td>Base Pointers:</td>
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<td></td>
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<tr>
<td>Peak Pointers:</td>
<td>64-bit</td>
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<tr>
<td>Other:</td>
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<tr>
<td>Power Management:</td>
<td>--</td>
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### Software

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</tr>
<tr>
<td>Power Management:</td>
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### CPU2017 License

- CPU2017 License: 9019
- Test Sponsor: Cisco Systems
- Tested by: Cisco Systems
- Hardware Availability: Apr-2019
- Software Availability: May-2019
- CPU Name: Intel Xeon Gold 5218
- Max MHz: 3900
- Nominal: 2300
- Enabled: 32 cores, 2 chips, 2 threads/core
- Orderable: 1,2 Chips
- Cache L1: 32 KB I + 32 KB D on chip per core
- L2: 1 MB I+D on chip per core
- L3: 22 MB I+D on chip per chip
- Other: None
- Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2666)
- Storage: 1 x 1.9 TB SSD SAS
- Other: None
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 5218, 2.30GHz)

SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
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<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
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<th>Seconds</th>
<th>Ratio</th>
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<tbody>
<tr>
<td>503.bwaves_r</td>
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<td>544.nab_r</td>
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<td>377</td>
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<td>549.fotonik3d_r</td>
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<td>554.rocks_r</td>
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<td>64</td>
<td>1162</td>
<td>107</td>
<td>1157</td>
<td>107</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
umactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 5218, 2.30GHz)

SPECrate®2017_fp_base = 178
SPECrate®2017_fp_peak = 180

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jun-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

General Notes (Continued)
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-senl Mon Jun 17 02:17:48 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 5218 CPU @ 2.30GHz
 2  "physical id"s (chips)
 64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
siblings : 32
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 64
On-line CPU(s) list: 0-63
Thread(s) per core: 2
Core(s) per socket: 16
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 5218 CPU @ 2.30GHz
Stepping: 6

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 5218, 2.30GHz)

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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Jun-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

### Platform Notes (Continued)

- CPU MHz: 2300.000
- CPU max MHz: 3900.0000
- CPU min MHz: 1000.0000
- BogoMIPS: 4600.00
- Virtualization: VT-x
- L1d cache: 32K
- L1i cache: 32K
- L2 cache: 1024K
- L3 cache: 22528K
- NUMA node0 CPU(s): 0-3,8-11,32-35,40-43
- NUMA node1 CPU(s): 4-7,12-15,36-39,44-47
- NUMA node2 CPU(s): 16-19,24-27,48-51,56-59
- NUMA node3 CPU(s): 20-23,28-31,52-55,60-63
- Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_patin mba tpr_shadow vmni flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 3dnowprefetch invpgid rdtscp mdrrsx mpxsr msr_rems invpcidid rtm cqm mpx rdঁt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsavec xsavec xnosaves cqm_llc cqm_occup_llc cqm_mbb/cm cqm_mbb/mem cqm_mbb/local ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni arch_capabilities ssbd

/proc/cpuinfo cache data

   cache size : 22528 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

- available: 4 nodes (0-3)
- node 0 cpus: 0 1 2 3 8 9 10 11 12 13 14 15 34 35 40 41 42 43
- node 0 size: 192103 MB
- node 0 free: 191750 MB
- node 1 cpus: 4 5 6 7 12 13 14 15 36 37 38 39 44 45 46 47
- node 1 size: 193527 MB
- node 1 free: 193194 MB
- node 2 cpus: 16 17 18 19 24 25 26 27 48 49 50 51 56 57 58 59
- node 2 size: 193498 MB
- node 2 free: 193284 MB
- node 3 cpus: 20 21 22 23 28 29 30 31 52 53 54 55 60 61 62 63
- node 3 size: 193526 MB
- node 3 free: 193176 MB
- node distances:
  - node 0 1 2 3
  - 0: 10 11 21 21

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 5218, 2.30GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECraten2017_fp_base = 178
SPECraten2017_fp_peak = 180

Test Date: Jun-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

1:  11  10  21  21
2:  21  21  10  11
3:  21  21  11  10

From /proc/meminfo
MemTotal:       791200096 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-senl 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Jun 17 02:04

SPEC is set to: /home/cpu2017
Filesystem   Type Size Used Avail Use% Mounted on
/dev/sda2     xfs  333G  59G  275G  18% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.4.0.4c.0.0411190411 04/11/2019
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2666

(End of data from sysinfo program)
**Cisco Systems**
Cisco UCS C240 M5 (Intel Xeon Gold 5218, 2.30GHz)

**Compiler Version Notes**

```
C
  519.lbm_r(base, peak) 538.imagick_r(base, peak)
  544.nab_r(base, peak)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++
  508.namd_r(base, peak) 510.parest_r(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++, C
  511.povray_r(base, peak) 526.blender_r(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++, C, Fortran
  507.cactuBSSN_r(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Fortran
  503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
  554.roms_r(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
```
**Cisco Systems**
Cisco UCS C240 M5 (Intel Xeon Gold 5218, 2.30GHz)

SPEC CPU®2017 Floating Point Rate Result

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Jun-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

**SPECrate®2017_fp_base = 178**  
**SPECrate®2017_fp_peak = 180**

---

**Compiler Version Notes (Continued)**

Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
Fortran, C      | 521.wrf_r(base, peak) 527.cam4_r(base, peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

**Base Compiler Invocation**

C benchmarks:  
`icc -m64 -std=c11`

C++ benchmarks:  
`icpc -m64`

Fortran benchmarks:  
`ifort -m64`

Benchmarks using both Fortran and C:  
`ifort -m64 icc -m64 -std=c11`

Benchmarks using both C and C++:  
`icpc -m64 icc -m64 -std=c11`

Benchmarks using Fortran, C, and C++:  
`icpc -m64 icc -m64 -std=c11 ifort -m64`

**Base Portability Flags**

503.bwaves_r: -DSPEC_LP64  
507.cactuBSSN_r: -DSPEC_LP64  
508.namd_r: -DSPEC_LP64  
510.parest_r: -DSPEC_LP64  
511.povray_r: -DSPEC_LP64  
519.lbm_r: -DSPEC_LP64

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 5218, 2.30GHz)  
SPECraten©2017_fp_base = 178
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CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
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Test Date: Jun-2019  
Hardware Availability: Apr-2019  
Software Availability: May-2019

Base Portability Flags (Continued)

521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

C++ benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11
**Cisco Systems**
Cisco UCS C240 M5 (Intel Xeon Gold 5218, 2.30GHz)  

**SPEC CPU®2017 Floating Point Rate Result**

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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Test Date:** Jun-2019  
**Tested by:** Cisco Systems  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

---

**Specify Compiler Invocation (Continued)**

C++ benchmarks:
```
icpc -m64
```

Fortran benchmarks:
```
ifort -m64
```

Benchmarks using both Fortran and C:
```
ifort -m64 icc -m64 -std=c11
```

Benchmarks using both C and C++:
```
icpc -m64 icc -m64 -std=c11
```

Benchmarks using Fortran, C, and C++:
```
icpc -m64 icc -m64 -std=c11 ifort -m64
```

---

**Peak Portability Flags**

Same as Base Portability Flags

---

**Peak Optimization Flags**

C benchmarks:
```
519.lbm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4
```
```
538.imagick_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4
```
```
544.nab_r: Same as 538.imagick_r
```

C++ benchmarks:
```
508.namd_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4
```
```
510.parest_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4
```

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 5218, 2.30GHz)

| SPECrate®2017_fp_base = 178 |
| SPECrate®2017_fp_peak = 180 |

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jun-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Peak Optimization Flags (Continued)

Fortran benchmarks:

503.bwaves_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

549.fotonik3d_r: Same as 503.bwaves_r

554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both Fortran and C:

-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both C and C++:

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

526.blender_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
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<tr>
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