### Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6238L, 2.10GHz)

<table>
<thead>
<tr>
<th>SpecTest</th>
<th>SPECrate\textsuperscript{\textregistered}2017_fp_peak</th>
<th>SPECrate\textsuperscript{\textregistered}2017_fp_base</th>
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</thead>
<tbody>
<tr>
<td>2017 FP</td>
<td>227</td>
<td>223</td>
</tr>
</tbody>
</table>

#### Hardware
- **CPU Name:** Intel Xeon Gold 6238L  
  - Max MHz: 3700  
  - Nominal: 2100  
  - Enabled: 44 cores, 2 chips, 2 threads/core  
  - Orderable: 1,2 Chips  
  - Cache L1: 32 KB I + 32 KB D on chip per core  
  - Cache L2: 1 MB I+D on chip per core  
  - Cache L3: 30.25 MB I+D on chip per core  
  - Other: None  
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)  
- **Storage:** 1 x 1.9 TB SSD SAS  
- **Other:** None

#### Software
- **OS:** SUSE Linux Enterprise Server 15 (x86_64)  
  - 4.12.14-23-default  
- **Compiler:**  
  - C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux  
  - Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux  
- **Parallel:** No  
- **Firmware:** Version 4.0.4d released May-2019  
- **File System:** xfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** 64-bit  
- **Other:** None  
- **Power Management:** --

<table>
<thead>
<tr>
<th>SpecTest</th>
<th>Copies</th>
<th>SPECrate\textsuperscript{\textregistered}2017_fp_base (223)</th>
<th>SPECrate\textsuperscript{\textregistered}2017_fp_peak (227)</th>
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<tbody>
<tr>
<td>503.bwaves_r</td>
<td>88</td>
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<tr>
<td>507.cactuBSSN_r</td>
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<td>508.namd_r</td>
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<td>510.parest_r</td>
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<td>511.povray_r</td>
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<td>554.roms_r</td>
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</table>
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6238L, 2.10GHz)

SPECrate®2017_fp_base = 223
SPECrate®2017_fp_peak = 227

## Results Table

<table>
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</tr>
</tbody>
</table>

SPECrate®2017_fp_base = 223
SPECrate®2017_fp_peak = 227

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.
For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6238L, 2.10GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECrater®2017_fp_base = 223
SPECrater®2017_fp_peak = 227

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

General Notes (Continued)

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-4.9t5 Tue Aug 6 19:38:03 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6238L CPU @ 2.10GHz
  2 "physical id"s (chips)
  88 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 22
siblings : 44
  physical 0: cores 0 1 2 3 4 5 8 9 10 11 12 16 17 18 19 20 21 24 25 26 27 28
  physical 1: cores 0 1 2 3 4 5 8 9 10 11 12 16 17 18 19 20 21 24 25 26 27 28

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 88
On-line CPU(s) list: 0-87
Thread(s) per core: 2
Core(s) per socket: 22
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6238L CPU @ 2.10GHz
Stepping: 7
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6238L, 2.10GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

SPECrate®2017_fp_base = 223
SPECrate®2017_fp_peak = 227

CPU MHz: 2100.000
CPU max MHz: 3700.0000
CPU min MHz: 1000.0000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 30976K
NUMA node0 CPU(s): 0-2, 6-8, 11-13, 17, 18, 44-46, 50-52, 55-57, 61, 62
NUMA node1 CPU(s): 3-5, 9, 10, 14-16, 19-21, 47-49, 53, 54, 58-60, 63-65
NUMA node2 CPU(s): 22-24, 28-30, 33-35, 39, 40, 66-68, 72-74, 77-79, 83, 84
NUMA node3 CPU(s): 25-27, 31, 32, 36-38, 41-43, 69-71, 75, 76, 80-82, 85-87
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtrm pcc l dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_l3 cdp_l3 invpcid_single intel_pmm mba tpr_shadow vni flexpriority ept
vpid fdgbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cmq mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsavevc xsaves cmqm llc cmq_occup_llc cmq_mbm_total cmq_mbm_local
ipbb ibrs stibp dtterm ida arat pln pts pku ospke avx512_vnni arch_capabilities ssbd

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 6 7 8 11 12 13 17 18 44 45 46 50 51 52 55 56 57 61 62
node 0 size: 192102 MB
node 0 free: 179247 MB
node 1 cpus: 3 4 5 9 10 14 15 16 19 20 21 47 48 49 53 54 58 59 60 63 64 65
node 1 size: 193526 MB
node 1 free: 184295 MB
node 2 cpus: 22 23 24 28 29 30 33 34 35 39 40 66 67 68 72 73 74 77 78 83 84
node 2 size: 193497 MB
node 2 free: 184296 MB
node 3 cpus: 25 26 27 31 32 36 37 38 41 42 43 69 70 71 75 76 80 81 82 85 86 87
node 3 size: 193524 MB
node 3 free: 184325 MB
node distances:
node 0 1 2 3
0: 10 11 21 21
1: 11 10 21 21

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6238L, 2.10GHz)

SPECrater®2017_fp_base = 223
SPECrater®2017_fp_peak = 227

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

2:  21  21  10  11
3:  21  21  11  10

From /proc/meminfo
MemTotal:       791194564 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
os-release:
  NAME="SLES"
  VERSION="15"
  VERSION_ID="15"
  PRETTY_NAME="SUSE Linux Enterprise Server 15"
  ID="sles"
  ID_LIKE="suse"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
  Linux linux-4vt5 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
  x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Aug 6 10:21

SPEC is set to: /home/cpu2017
  Filesystem    Type  Size  Used Avail Use% Mounted on
  /dev/sda1      xfs   224G  56G  168G  25% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
  BIOS Cisco Systems, Inc. C240M5.4.0.4d.0.0506190827 05/06/2019
  Memory:
  24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6238L, 2.10GHz)  

**Compiler Version Notes**

```
C               | 519.lbm_r(base, peak) 538.imagick_r(base, peak)  
| 544.nab_r(base, peak)  

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  

C++             | 508.namd_r(base, peak) 510.parest_r(base, peak)  

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  

C++, C          | 511.povray_r(base, peak) 526.blender_r(base, peak)  

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  

C++, C, Fortran | 507.cactuBSSN_r(base, peak)  

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  

Fortran         | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)  
| 554.roms_r(base, peak)  

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
(Continued on next page)
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SPECrate®2017_fp_base = 223
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Compiler Version Notes (Continued)

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--------------------------------------------------------------------------------
Fortran, C      | 521.wrf_r(base, peak) 527.cam4_r(base, peak)
--------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64

(Continued on next page)
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Test Sponsor: Cisco Systems  
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Test Date: Aug-2019  
Hardware Availability: Apr-2019  
Software Availability: May-2019

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### Base Portability Flags (Continued)

521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

---

### Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

C++ benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

---

### Peak Compiler Invocation

C benchmarks:
cc -m64 -std=c11

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(Continued on next page)
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Cisco UCS C240 M5 (Intel Xeon Gold 6238L, 2.10GHz)

SPECrate®2017_fp_base = 223
SPECrate®2017_fp_peak = 227

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Peak Compiler Invocation (Continued)

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags
Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
519.lbm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

538.imagick_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

544.nab_r: Same as 538.imagick_r

C++ benchmarks:
508.namd_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

510.parest_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

(Continued on next page)
### Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6238L, 2.10GHz)

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<th>SPECrate®2017_fp_base = 223</th>
<th>Test Date: Aug-2019</th>
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<td>SPECrate®2017_fp_peak = 227</td>
<td>Hardware Availability: Apr-2019</td>
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<td>Software Availability: May-2019</td>
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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

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**Peak Optimization Flags (Continued)**

**Fortran benchmarks:**

503.bwaves_r:  
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4 -auto  
-nostandard-realloc-lhs -align array32byte

549.fotonik3d_r: Same as 503.bwaves_r

554.roms_r:  
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512  
-03 -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs  
-align array32byte

**Benchmarks using both Fortran and C:**

-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3  
-no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs  
-align array32byte

**Benchmarks using both C and C++:**

511.povray_r:  
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512  
-03 -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=4

526.blender_r:  
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4

**Benchmarks using Fortran, C, and C++:**

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4 -auto  
-nostandard-realloc-lhs -align array32byte

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The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:


## SPEC CPU®2017 Floating Point Rate Result

**Cisco Systems**  
Cisco UCS C240 M5 (Intel Xeon Gold 6238L, 2.10GHz)

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| Test Date:           | Aug-2019              |
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Tested with SPEC CPU®2017 v1.0.5 on 2019-08-06 10:08:02-0400.  
Originally published on 2019-09-06.