**Cisco Systems**
Cisco UCS B200 M5 (Intel Xeon Gold 6244, 3.60GHz)

<table>
<thead>
<tr>
<th>Software</th>
<th>Hardware</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>OS:</strong> SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default</td>
<td><strong>CPU Name:</strong> Intel Xeon Gold 6244</td>
</tr>
<tr>
<td>Compiler: C/C++: Version 19.0.1.144 of Intel C/C++ Compiler Build 20181018 for Linux; Fortran: Version 19.0.1.144 of Intel Fortran Compiler Build 20181018 for Linux</td>
<td><strong>Max MHz:</strong> 4400</td>
</tr>
<tr>
<td><strong>Compiler:</strong> No</td>
<td><strong>Nominal:</strong> 3600</td>
</tr>
<tr>
<td>Firmware: Version 4.0.4b released Apr-2019</td>
<td><strong>Enabled:</strong> 16 cores, 2 chips, 2 threads/core</td>
</tr>
<tr>
<td>File System: btrfs</td>
<td><strong>Orderable:</strong> 1,2 chips</td>
</tr>
<tr>
<td>System State: Run level 3 (multi-user)</td>
<td><strong>Cache L1:</strong> 32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>Base Pointers: 64-bit</td>
<td><strong>L2:</strong> 1 MB I+D on chip per core</td>
</tr>
<tr>
<td>Peak Pointers: Not Applicable</td>
<td><strong>L3:</strong> 24.75 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Other: None</td>
<td><strong>Other:</strong> None</td>
</tr>
<tr>
<td>Power Management: --</td>
<td><strong>Memory:</strong> 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)</td>
</tr>
</tbody>
</table>

| **Test Sponsor:** Cisco Systems | **Test Date:** Aug-2019 |
| **Tested by:** Cisco Systems | **Hardware Availability:** Apr-2019 |

<table>
<thead>
<tr>
<th><strong>Test Date:</strong> Aug-2019</th>
<th><strong>Software Availability:</strong> May-2019</th>
</tr>
</thead>
</table>

**SPEC CPU®2017 Floating Point Rate Result**

**SPECrate®2017_fp_base = 148**

**SPECrate®2017_fp_peak = Not Run**
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6244, 3.60GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECrate®2017_fp_base = 148
SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>32</td>
<td>712</td>
<td>451</td>
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<td>451</td>
<td>711</td>
<td>451</td>
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<tr>
<td>507.cactuBSSN_r</td>
<td>32</td>
<td>431</td>
<td>94.0</td>
<td>431</td>
<td>94.0</td>
<td>433</td>
<td>93.6</td>
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<tr>
<td>508.namd_r</td>
<td>32</td>
<td>304</td>
<td>100</td>
<td>304</td>
<td>99.9</td>
<td>302</td>
<td>101</td>
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<tr>
<td>510.parest_r</td>
<td>32</td>
<td>779</td>
<td>107</td>
<td>780</td>
<td>107</td>
<td>782</td>
<td>107</td>
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<tr>
<td>511.povray_r</td>
<td>32</td>
<td>506</td>
<td>148</td>
<td>507</td>
<td>147</td>
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<td>148</td>
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<tr>
<td>519.lbm_r</td>
<td>32</td>
<td>386</td>
<td>87.4</td>
<td>386</td>
<td>87.5</td>
<td>386</td>
<td>87.4</td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>32</td>
<td>415</td>
<td>173</td>
<td>410</td>
<td>175</td>
<td>410</td>
<td>175</td>
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<tr>
<td>526.blender_r</td>
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<td>358</td>
<td>136</td>
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<td>136</td>
<td>359</td>
<td>136</td>
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<tr>
<td>527.cam4_r</td>
<td>32</td>
<td>362</td>
<td>155</td>
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<td>150</td>
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<tr>
<td>538.imagick_r</td>
<td>32</td>
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<td>306</td>
<td>261</td>
<td>305</td>
<td>260</td>
<td>306</td>
</tr>
<tr>
<td>544.nab_r</td>
<td>32</td>
<td>249</td>
<td>216</td>
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<td>216</td>
<td>246</td>
<td>219</td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>32</td>
<td>994</td>
<td>125</td>
<td>992</td>
<td>126</td>
<td>996</td>
<td>125</td>
</tr>
<tr>
<td>554.roms_r</td>
<td>32</td>
<td>535</td>
<td>95.1</td>
<td>536</td>
<td>94.8</td>
<td>538</td>
<td>94.5</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"
Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6244, 3.60GHz)

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
<th>Test Date:</th>
<th>Aug-2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
<td>Hardware Availability:</td>
<td>Apr-2019</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
<td>Software Availability:</td>
<td>May-2019</td>
</tr>
</tbody>
</table>

**General Notes (Continued)**
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

**Platform Notes**

BIOS Settings:
- Intel HyperThreading Technology set to Enabled
- CPU performance set to Enterprise
- Power Performance Tuning set to OS Controls
- SNC set to Disabled
- IMC Interleaving set to Auto
- Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-db10 Sat Aug 17 12:10:04 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
- model name: Intel(R) Xeon(R) Gold 6244 CPU @ 3.60GHz
- 2 "physical id"s (chips)
- 32 "processors"
- cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
- cpu cores : 8
- siblings : 16
- physical 0: cores 1 4 9 17 18 19 25 27
- physical 1: cores 2 3 4 17 18 24 25 27

From lscpu:
- Architecture: x86_64
- CPU op-mode(s): 32-bit, 64-bit
- Byte Order: Little Endian
- CPU(s): 32
- On-line CPU(s) list: 0-31
- Thread(s) per core: 2
- Core(s) per socket: 8
- Socket(s): 2
- NUMA node(s): 4
- Vendor ID: GenuineIntel
- CPU family: 6
- Model: 85

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6244, 3.60GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

SPECrate®2017_fp_base = 148
SPECrate®2017_fp_peak = Not Run

Model name: Intel(R) Xeon(R) Gold 6244 CPU @ 3.60GHz
Stepping: 6
CPU MHz: 3600.000
CPU max MHz: 4400.0000
CPU min MHz: 1200.0000
BogoMIPS: 7200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 25344K
NUMA node0 CPU(s): 0,2,3,6,16,18,19,22
NUMA node1 CPU(s): 1,4,5,7,17,20,21,23
NUMA node2 CPU(s): 8,11,13,14,24,27,29,30
NUMA node3 CPU(s): 9,10,12,15,25,26,28,31
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref perf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdmb fma cx16 xtpr pdcache pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_l3 cdp_l3 invpcid_single intel_pwpin mba tpr_shadow vmmi flexpriority ept
vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erva cmp1 idt tscinvvd msr rdtscp
rtm qm xsaveopt xsave xsaveopt xsaves cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_domain
ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_kpg_req kpu
ospke avx512_vnni arch_capabilities ssbd

/platform/cpupower --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.

Warning: running out of cache data

cache size : 25344 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.

Warning: running out of cache data

cache size : 25344 KB

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6244, 3.60GHz)

SPECrate®2017_fp_base = 148
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Software Availability: May-2019

Platform Notes (Continued)

node  0  1  2  3
 0: 10 11 21 21
 1: 11 10 21 21
 2: 21 21 10 11
 3: 21 21 11 10

From /proc/meminfo
MemTotal: 791013836 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
os-release:
  NAME="SLES"
  VERSION="15"
  VERSION_ID="15"
  PRETTY_NAME="SUSE Linux Enterprise Server 15"
  ID="sles"
  ID_LIKE="suse"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-db10 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Aug 17 08:55

SPEC is set to: /home/cpu2017
  Filesystem  Type  Size  Used  Avail  Use%  Mounted on
  /dev/sdc2    btrfs  222G  59G  163G  27%  /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
  BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
  Memory:
  24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6244, 3.60GHz)

SPECrater®2017_fp_base = 148
SPECrater®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)
(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C               | 519.ibm_r(base) 538.imagick_r(base) 544.nab_r(base)
-------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
   Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
-------------------------------------------------------------------------------

==============================================================================
C++             | 508.namd_r(base) 510.parest_r(base)
-------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
   Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
-------------------------------------------------------------------------------

==============================================================================
C++, C          | 511.povray_r(base) 526.blender_r(base)
-------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
   Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
   Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
-------------------------------------------------------------------------------

==============================================================================
C++, C, Fortran | 507.cactusBSSN_r(base)
-------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
   Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
   Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
   64, Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
-------------------------------------------------------------------------------

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Cisco Systems
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SPECraten%2017_fp_base = 148
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CPU2017 License: 9019
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Compiler Version Notes (Continued)

<table>
<thead>
<tr>
<th>Fortran</th>
<th>503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)</th>
</tr>
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<tbody>
<tr>
<td>Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.1.144 Build 20181018</td>
<td></td>
</tr>
<tr>
<td>Copyright (C) 1985–2018 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
</tbody>
</table>

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64

(Continued on next page)
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Base Portability Flags (Continued)

510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

C++ benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

The flags files that were used to format this result can be browsed at
Cisco Systems  
Cisco UCS B200 M5 (Intel Xeon Gold 6244, 3.60GHz)  

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<tr>
<th>SPECrate®2017_fp_base</th>
<th>148</th>
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<tbody>
<tr>
<td>SPECrate®2017_fp_peak</td>
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</tr>
</tbody>
</table>

CPU2017 License: 9019
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Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

You can also download the XML flags sources by saving the following links:

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Tested with SPEC CPU®2017 v1.0.5 on 2019-08-17 15:10:03-0400.
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