### SPEC CPU®2017 Integer Rate Result

**Cisco Systems**

Cisco UCS B200 M5 (Intel Xeon Silver 4210, 2.20GHz)

- **SPECrate®2017_int_base = 108**
- **SPECrate®2017_int_peak = Not Run**

<table>
<thead>
<tr>
<th>Copies</th>
<th>SPECrate®2017_int_base (108)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
<tr>
<td>500.perlbench_r</td>
<td>40</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>40</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>40</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>40</td>
</tr>
<tr>
<td>523.xalancbk_r</td>
<td>40</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>40</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>40</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>40</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>40</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>40</td>
</tr>
</tbody>
</table>

### Hardware

- **CPU Name:** Intel Xeon Silver 4210
- **Max MHz:** 3200
- **Nominal:** 2200
- **Enabled:** 20 cores, 2 chips, 2 threads/core
- **Orderable:** 1.2 chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **Cache L2:** 1 MB I+D on chip per core
- **Cache L3:** 13.75 MB I+D on chip per chip
- **Other:** None
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2400)
- **Storage:** 1 x 1.2 TB SAS 7.2K RPM
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 15 (x86_64)
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler Build 20190416 for Linux;
  Fortran: Version 19.0.4.227 of Intel Fortran Compiler Build 20190416 for Linux
- **Parallel:** No
- **Firmware:** Version 4.0.4b released Apr-2019
- **File System:** btrfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** None
- **Power Management:** --
SPEC CPU®2017 Integer Rate Result

Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4210, 2.20GHz)

Copyright 2017-2020 Standard Performance Evaluation Corporation

SPECrate®2017_int_base = 108
SPECrate®2017_int_peak = Not Run

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>perfbench_r</td>
<td>40</td>
<td>764</td>
<td><strong>83.3</strong></td>
<td>766</td>
<td>83.1</td>
<td>763</td>
<td>83.5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>gcc_r</td>
<td>40</td>
<td>649</td>
<td><strong>87.3</strong></td>
<td>655</td>
<td>86.4</td>
<td>646</td>
<td>87.7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>mcf_r</td>
<td>40</td>
<td>450</td>
<td>144</td>
<td>452</td>
<td>143</td>
<td><strong>450</strong></td>
<td><strong>144</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>omnetpp_r</td>
<td>40</td>
<td>744</td>
<td>70.6</td>
<td><strong>744</strong></td>
<td><strong>70.5</strong></td>
<td>745</td>
<td>70.4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>xalancblk_r</td>
<td>40</td>
<td>355</td>
<td>119</td>
<td>354</td>
<td>119</td>
<td><strong>355</strong></td>
<td><strong>119</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>x264_r</td>
<td>40</td>
<td>744</td>
<td>70.6</td>
<td><strong>744</strong></td>
<td><strong>70.5</strong></td>
<td>745</td>
<td>70.4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>deepsjeng_r</td>
<td>40</td>
<td>501</td>
<td>91.5</td>
<td><strong>501</strong></td>
<td><strong>91.5</strong></td>
<td>501</td>
<td>91.5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>leela_r</td>
<td>40</td>
<td>791</td>
<td>83.7</td>
<td><strong>791</strong></td>
<td><strong>83.8</strong></td>
<td>790</td>
<td>83.8</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>exchange2_r</td>
<td>40</td>
<td>472</td>
<td>222</td>
<td><strong>472</strong></td>
<td><strong>222</strong></td>
<td>474</td>
<td>221</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>xz_r</td>
<td>40</td>
<td>603</td>
<td>71.7</td>
<td><strong>602</strong></td>
<td><strong>71.7</strong></td>
<td>602</td>
<td>71.7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

SPECrate®2017_int_base = 108
SPECrate®2017_int_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Silver 4210, 2.20GHz)

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
</tbody>
</table>

| SPECraten 2017_int_base = | 108 |
| SPECraten 2017_int_peak = | Not Run |

**Test Date:** Aug-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

### General Notes (Continued)

is mitigated in the system as tested and documented.

### Platform Notes

- **BIOS Settings:**
  - Intel HyperThreading Technology set to Enabled
  - CPU performance set to Enterprise
  - Power Performance Tuning set to OS Controls
  - SNC set to Enabled
  - IMC Interleaving set to 1-way Interleave
  - Patrol Scrub set to Disabled
  - Sysinfo program /home/cpu2017/bin/sysinfo

- **Rev:** r5797 of 2017-06-14 96c45e4568ad54c135fd618bcb091c0f

- **Running on:** linux-5vrl Sat Aug 24 06:53:27 2019

**SUT (System Under Test) info as seen by some common utilities.**

For more information on this section, see  
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

**From /proc/cpuinfo**

- model name : Intel(R) Xeon(R) Silver 4210 CPU @ 2.20GHz
- 2 "physical id"s (chips)
- 40 "processors"

- cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

  - cpu cores : 10
  - siblings : 20
  - physical 0: cores 0 1 2 3 4 8 9 10 11 12
  - physical 1: cores 0 1 2 3 4 8 9 10 11 12

**From lscpu:**

- Architecture: x86_64
- CPU op-mode(s): 32-bit, 64-bit
- Byte Order: Little Endian
- CPU(s): 40
- On-line CPU(s) list: 0-39
- Thread(s) per core: 2
- Core(s) per socket: 10
- Socket(s): 2
- NUMA node(s): 2
- Vendor ID: GenuineIntel
- CPU family: 6
- Model: 85
- Model name: Intel(R) Xeon(R) Silver 4210 CPU @ 2.20GHz
- Stepping: 6
- CPU MHz: 2200.000

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4210, 2.20GHz)

SPECrater®2017_int_base = 108
SPECrater®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

CPU max MHz: 3200.0000
CPU min MHz: 1000.0000
BogoMIPS: 4400.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 14080K
NUMA node0 CPU(s): 0-9,20-29
NUMA node1 CPU(s): 10-19,30-39

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt

tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_13 cdp_13 invpcid_single intel_pinn mba tpr_shadow vmmi flexpriority ept

tpm fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 뿐ינ.cid rtm cqm mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl

/proc/cpuinfo cache data

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.

available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 20 21 22 23 24 25 26 27 28 29
node 0 size: 386531 MB
node 0 free: 386030 MB
node 1 cpus: 10 11 12 13 14 15 16 17 18 19 30 31 32 33 34 35 36 37 38 39
node 1 size: 387044 MB
node 1 free: 386600 MB
node distances:

From /proc/meminfo

MemTotal: 792142344 kB

HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release*/etc/*version*/
os-release:

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4210, 2.20GHz)

SPECrater®2017_int_base = 108
SPECrater®2017_int_peak = Not Run

Test Date:     Aug-2019
Hardware Availability:  Apr-2019
Software Availability:  May-2019

CPU2017 License:  9019
Test Sponsor:  Cisco Systems
Tested by:  Cisco Systems

Platform Notes (Continued)

NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-5vrl 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Aug 24 06:45
SPEC is set to:  /home/cpu2017
Filesystem     Type   Size  Used Avail Use% Mounted on
/dev/sdb1      btrfs  224G   15G  208G   7% /home

Additional information from dmidecode follows.  WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400

Compiler Version Notes

==============================================================================
<table>
<thead>
<tr>
<th>C</th>
<th>500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>525.x264_r(base) 557.xz_r(base)</td>
</tr>
</tbody>
</table>
==============================================================================

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
<table>
<thead>
<tr>
<th>C++</th>
<th>520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>541.leela_r(base)</td>
</tr>
</tbody>
</table>
==============================================================================

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4210, 2.20GHz)

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

SPECrate®2017_int_base = 108
SPECrate®2017_int_peak = Not Run

Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4210, 2.20GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Compiler Version Notes (Continued)
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---

Fortran | 548.exchange2_r(base)
---

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4210, 2.20GHz)

SPECrate®2017_int_base = 108
SPECrate®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Base Optimization Flags (Continued)

C benchmarks (continued):
- lqkmalloc

C++ benchmarks:
- Wl, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- qopt-mem-layout-trans=4
- /usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
- lqkmalloc

Fortran benchmarks:
- Wl, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
- /usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
- lqkmalloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2019-08-24 09:53:26-0400.
Report generated on 2020-07-02 18:04:06 by CPU2017 PDF formatter v6255.
Originally published on 2019-09-19.