Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5222, 3.80GHz)

**SPECspeed®2017_fp_base = 57.9**
**SPECspeed®2017_fp_peak = Not Run**

<table>
<thead>
<tr>
<th>Test Date:</th>
<th>Aug-2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardware Availability:</td>
<td>Apr-2019</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>May-2019</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019
**Test Sponsor:** Cisco Systems
**Tested by:** Cisco Systems

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### Hardware

- **CPU Name:** Intel Xeon Gold 5222
- **Max MHz:** 3900
- **Nominal:** 3800
- **Enabled:** 8 cores, 2 chips
- **Orderable:** 1,2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **Cache L2:** 1 MB I+D on chip per core
- **Cache L3:** 16.5 MB I+D on chip per chip
- **Other:** None
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2934)
- **Storage:** 1 x 600G SAS 10K RPM
- **Other:** None

- **OS:** SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 4.0.4b released Apr-2019
- **File System:** btrfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** None
- **Power Management:** --

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**Threads**

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Value</th>
<th>SPECspeed®2017_fp_base (57.9)</th>
</tr>
</thead>
<tbody>
<tr>
<td>603.bwaves_s</td>
<td>8</td>
<td>54.8</td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
<td>8</td>
<td>54.8</td>
</tr>
<tr>
<td>619.lbm_s</td>
<td>8</td>
<td>46.8</td>
</tr>
<tr>
<td>621.wrf_s</td>
<td>8</td>
<td>61.1</td>
</tr>
<tr>
<td>627.cam4_s</td>
<td>8</td>
<td>29.7</td>
</tr>
<tr>
<td>628.pop2_s</td>
<td>8</td>
<td>46.7</td>
</tr>
<tr>
<td>638.imagick_s</td>
<td>8</td>
<td>36.7</td>
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<tr>
<td>644.nab_s</td>
<td>8</td>
<td>64.5</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>8</td>
<td>56.4</td>
</tr>
<tr>
<td>654.roms_s</td>
<td>8</td>
<td>55.2</td>
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SPECSpeed®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
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Test Date: Aug-2019
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Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
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<th>Seconds</th>
<th>Ratio</th>
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</thead>
<tbody>
<tr>
<td>603.bwaves_s</td>
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<tr>
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<td>649.fotonik3d_s</td>
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<td>284</td>
<td>55.4</td>
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<td>285</td>
<td>55.2</td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
Memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
SNC set to Disabled

(Continued on next page)
Cisco Systems
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<td>Not Run</td>
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</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

IMC Interleaving set to Auto
Patrol Scrub set to Disabled
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-k1c6 Sat Aug 24 21:08:24 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name: Intel(R) Xeon(R) Gold 5222 CPU @ 3.80GHz
  2 "physical id"s (chips)
  8 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores: 4
siblings: 4
physical 0: cores 5 8 9 13
physical 1: cores 2 5 9 13

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 8
On-line CPU(s) list: 0-7
Thread(s) per core: 1
Core(s) per socket: 4
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 5222 CPU @ 3.80GHz
Stepping: 6
CPU MHz: 3800.000
CPU max MHz: 3900.0000
CPU min MHz: 1200.0000
BogoMIPS: 7600.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 16896K
NUMA node0 CPU(s): 0-3
NUMA node1 CPU(s): 4-7

(Continued on next page)
Cisco Systems
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Platform Notes (Continued)

Flags:          fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
                pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdelgb rdtsscp
                lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
                aperfmperf tsc_known_freq pni pclmulqdq dtex64 monitor ds_cpl vmx smx est tm2 ssse3
                sdbg fma cx16 xtpm pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
                tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
                epb cat_13 cmp_13 invpcid_single intel_puin mba tpr_shadow vmni flexpriority ept
                vpid fsqgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
                avx512f avx512dq rdseed adx smap clfushopt clwb intel_pt avx512cd avx512bw avx512vl
                xsaveopt xsave xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local
                ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
                ospke avx512_vnni arch_capabilities ssbd

/cacheinfo cache data
  cache size : 16896 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3
  node 0 size: 385460 MB
  node 0 free: 380771 MB
  node 1 cpus: 4 5 6 7
  node 1 size: 387018 MB
  node 1 free: 382238 MB

node distances:
  node  0  1
  0:  10  21
  1:  21  10

From /proc/meminfo
  MemTotal:       791018772 kB
  HugePages_Total:       0
  Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15"
    VERSION_ID="15"
    PRETTY_NAME="SUSE Linux Enterprise Server 15"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15"

  uname -a:

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Platform Notes (Continued)
Linux linux-klc6 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux
run-level 3 Aug 24 13:54
SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sdc2 btrfs 557G 22G 535G 4% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.04071258 04/07/2019
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes
==============================================================================
C               | 619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
==============================================================================
C++, C, Fortran | 607.cactuBSSN_s(base)
==============================================================================
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
Fortran         | 603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)

(Continued on next page)
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Compiler Version Notes (Continued)
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation
C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags
603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64
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### Base Optimization Flags

**C benchmarks:**
- `xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`
- `ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP`

**Fortran benchmarks:**
- `DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`
- `ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp`
- `nostandard-realloc-lhs`

**Benchmarks using both Fortran and C:**
- `xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`
- `ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP`
- `nostandard-realloc-lhs`

**Benchmarks using Fortran, C, and C++:**
- `xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`
- `ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP`
- `nostandard-realloc-lhs`

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:

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