Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6242, 2.80GHz)

SPECratio®2017_fp_base = 199
SPECratio®2017_fp_peak = Not Run

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**Hardware**

- **CPU Name:** Intel Xeon Gold 6242
- **Max MHz:** 3900
- **Nominal:** 2800
- **Enabled:** 32 cores, 2 chips, 2 threads/core
- **Orderable:** 1,2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 22 MB I+D on chip per chip
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
- **Storage:** 1 x 600 GB 10K RPM SAS
- **Other:** None

**Software**

- **OS:** SUSE Linux Enterprise Server 15 (x86_64)
- **Compiler:** C/C++; Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
- **Fortran:** Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** No
- **Firmware:** Version 4.0.4b released Apr-2019
- **File System:** btrfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** None
- **Power Management:** --
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6242, 2.80GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECraten2017_fp_base = 199
SPECraten2017_fp_peak = Not Run

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

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**Submit Notes**

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

**General Notes**

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
  sync; echo 3>
  /proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6242, 2.80GHz)

SPECrater 2017_fp_base = 199
SPECrater 2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

General Notes (Continued)
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-k1c6 Mon Aug 26 22:57:31 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
  model name : Intel(R) Xeon(R) Gold 6242 CPU @ 2.80GHz
  2  "physical id"s (chips)
  64 "processors"
  cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 16
  siblings : 32
  physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
  physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu:
  Architecture:           x86_64
  CPU op-mode(s):         32-bit, 64-bit
  Byte Order:             Little Endian
  CPU(s):                 64
  On-line CPU(s) list:    0-63
  Thread(s) per core:     2
  Core(s) per socket:     16
  Socket(s):              2
  NUMA node(s):           4
  Vendor ID:              GenuineIntel
  CPU family:             6
  Model:                  85

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6242, 2.8GHz)

SPECratenot set = 199
SPECratenot peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Aug-2019
Hardware Availability: Apr-2019
Tested by: Cisco Systems
Software Availability: May-2019

Platform Notes (Continued)

Model name: Intel(R) Xeon(R) Gold 6242 CPU @ 2.80GHz
Stepping: 6
CPU MHz: 2800.00
CPU max MHz: 3900.0000
CPU min MHz: 1200.0000
BogoMIPS: 5600.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 22528K
NUMA node0 CPU(s): 0-3,8-11,32-35,40-43
NUMA node1 CPU(s): 4-7,12-15,36-39,44-47
NUMA node2 CPU(s): 16-19,24-27,48-51,56-59
NUMA node3 CPU(s): 20-23,28-31,52-55,60-63
Flags: fpu vme de pse ts cmov pat pse36 clflush dts iommu pdm nonstop_tsc arch_perfmon smep aes xsave avx f16c rdrand lahf_lm abm 3nowprefetch cpuid_fault ebp cat_13 cdp_13 invpcid_single intel_pinnable tpr_shadow vmx flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 3dnowprefetch invpcid rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512bw avx512vl xsaveopt xsaveopt xsaveprec xsave xmlist vmxset cr4vpcl律师事务 contemplated ssbd

/proc/cpuinfo cache data
  cache size : 22528 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 4 nodes (0-3)
  node 0 cpus: 0 1 2 3 8 9 10 11 32 33 34 35 40 41 42 43
  node 0 size: 191903 MB
  node 0 free: 186493 MB
  node 1 cpus: 4 5 6 7 12 13 14 15 36 37 38 39 44 45 46 47
  node 1 size: 193522 MB
  node 1 free: 189726 MB
  node 2 cpus: 16 17 18 19 24 25 26 27 48 49 50 51 56 57 58 59
  node 2 size: 193522 MB
  node 2 free: 189829 MB
  node 3 cpus: 20 21 22 23 28 29 30 31 52 53 54 55 60 61 62 63
  node 3 size: 193519 MB
  node 3 free: 189768 MB
  node distances:
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6242, 2.80GHz)

SPECrate®2017_fp_base = 199
SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

node  0   1   2   3
 0:  10  11  21  21
 1:  11  10  21  21
 2:  21  21  10  11
 3:  21  21  11  10

From /proc/meminfo
MemTotal:       791007672 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

From /etc/*release*/etc/*version*
os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-k1c6 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Aug 26 17:14

SPEC is set to: /home/cpu2017
Filesystem     Type   Size  Used Avail Use% Mounted on
/dev/sdc2      btrfs  557G   29G  528G   6% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
Memory:
  24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

C               | 519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6242, 2.80GHz)

SPECrater®2017_fp_base = 199
SPECrater®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Compiler Version Notes (Continued)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

-----------------------------------------------------------------------------
C++ | 508.namd_r(base) 510.parest_r(base)
-----------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

-----------------------------------------------------------------------------
C++, C | 511.povray_r(base) 526.blender_r(base)
-----------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

-----------------------------------------------------------------------------
C++, C, Fortran | 507.cactuBSSN_r(base)
-----------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

-----------------------------------------------------------------------------
Fortran | 503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)
-----------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6242, 2.80GHz)

SPECratenot run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Compiler Version Notes (Continued)

Fortran, C | 521.wrf_r(base) 527.cam4_r(base)

Intel (R) Fortran Intel (R)64 Compiler for applications running on Intel (R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel (R) C Intel (R)64 Compiler for applications running on Intel (R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

503.bwaves_r: -DSPEC LP64
507.cactuBSSN_r: -DSPEC LP64
508.namd_r: -DSPEC LP64
510.parest_r: -DSPEC LP64
511.povray_r: -DSPEC LP64
519.ibm_r: -DSPEC LP64
521.wrf_r: -DSPEC LP64 -DSPEC CASE FLAG -convert big_endian
526.blender_r: -DSPEC LP64 -DSPEC LINUX -funsigned-char
527.cam4_r: -DSPEC LP64 -DSPEC CASE FLAG
538.imagick_r: -DSPEC LP64

(Continued on next page)
SPEC CPU®2017 Floating Point Rate Result

Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6242, 2.80GHz)

SPECrade®2017_fp_base = 199
SPECrade®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Base Portability Flags (Continued)

544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

C++ benchmarks:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6242, 2.80GHz)

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
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Test Date: Aug-2019
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Software Availability: May-2019

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2019-08-27 01:57:30-0400.
Originally published on 2019-09-19.