**Cisco Systems**  
Cisco UCS B200 M5 (Intel Xeon Gold 6240, 2.60GHz)  

***SPECspeed®2017_fp_base = 131***  
***SPECspeed®2017_fp_peak = Not Run***

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
<th>Test Date:</th>
<th>Aug-2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
<td>Hardware Availability:</td>
<td>Apr-2019</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
<td>Software Availability:</td>
<td>May-2019</td>
</tr>
</tbody>
</table>

### Hardware

- **CPU Name:** Intel Xeon Gold 6240
- **Max MHz:** 3900
- **Nominal:** 2600
- **Enabled:** 36 cores, 2 chips
- **Orderable:** 1,2 Chips
- **Cache L1:** 32 KB I+D on chip per core
- **Cache L2:** 1 MB I+D on chip per core
- **Cache L3:** 24.75 MB I+D on chip per chip
- **Other:** None
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
- **Storage:** 1 x 240 GB M.2 SATA SSD
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 15 (x86_64)
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 4.0.4b released Apr-2019
- **File System:** btrfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** None
- **Power Management:** --
## Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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</tbody>
</table>

**SPECspeed®2017_fp_base = 131**

**SPECspeed®2017_fp_peak = Not Run**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### General Notes

Environment variables set by runcpu before the start of the run:

LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM

memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

sync; echo 3> /proc/sys/vm/drop_caches

runcpu command invoked through numactl i.e.:

numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

### Platform Notes

BIOS Settings:

Intel HyperThreading Technology set to Disabled

SNC set to Disabled

(Continued on next page)
Cisco Systems
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Platform Notes (Continued)

Power Performance Tuning set to OS Controls
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcd08f2999c33d61f64985e45859ea9
running on linux-db10 Sat Aug 31 17:35:22 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6240 CPU @ 2.60GHz
  2 "physical id"s (chips)
  36 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 18
siblings : 18
physical 0: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
physical 1: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 36
On-line CPU(s) list: 0-35
Thread(s) per core: 1
Core(s) per socket: 18
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6240 CPU @ 2.60GHz
Stepping: 6
CPU MHz: 2600.000
CPU max MHz: 3900.0000
CPU min MHz: 1000.0000
BogoMIPS: 5200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 25344K
NUMA node0 CPU(s): 0-17
NUMA node1 CPU(s): 18-35

(Continued on next page)
SPEC CPU®2017 Floating Point Speed Result

Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6240, 2.60GHz)

CPU2017 License: 9019
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Platform Notes (Continued)

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpelgb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nop1 xtopology nonstop_tsc cpuid
aperfmpref tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtrr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt

tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_l3 cdp_l3 invpcid_single intel_ppin mba tpr_shadow vmni flexpriority ept
vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
avx512f avx512dq rdseed adx clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaves optx xsave xaxx xsaveopt xsavec xsaveopt xsaveopt xsaveopt xsaveopt xsaveopt

/proc/cpuinfo cache data

cache size : 25344 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.

available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
node 0 size: 385428 MB
node 0 free: 382961 MB
node 1 cpus: 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35
node 1 size: 387045 MB
node 1 free: 379819 MB
node distances:
node 0 1
0: 10 21
1: 21 10

From /proc/meminfo

MemTotal: 791013400 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*

os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:

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Platform Notes (Continued)

Linux linux-db10 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: _user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW
run-level 3 Aug 31 12:02
SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sdc2 btrfs 222G 58G 164G 27% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

Compiler Version Notes

==============================================================================
| C                        | 619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base) |
|----------------------------|
| Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, |
| Version 19.0.4.227 Build 20190416 |
| Copyright (C) 1985–2019 Intel Corporation. All rights reserved. |

==============================================================================
| C++, C, Fortran           | 607.cactuBSSN_s(base) |
|----------------------------|
| Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, |
| Version 19.0.4.227 Build 20190416 |
| Copyright (C) 1985–2019 Intel Corporation. All rights reserved. |
| Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, |
| Version 19.0.4.227 Build 20190416 |
| Copyright (C) 1985–2019 Intel Corporation. All rights reserved. |
| Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) |

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Cisco Systems
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### SPEC CPU 2017 Floating Point Speed Result

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### Compiler Version Notes (Continued)

```
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
```

---

**Fortran**  
| 603.bwaves_s(base) | 649.fotonik3d_s(base) | 654.roms_s(base) |
---

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

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**Fortran, C**  
| 621.wrf_s(base) | 627.cam4_s(base) | 628.pop2_s(base) |
---

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.0.4.227 Build 20190416  
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### Base Compiler Invocation

**C benchmarks:**
`
icc -m64 -std=c11
`

**Fortran benchmarks:**
`
ifort -m64
`

**Benchmarks using both Fortran and C:**
`
ifort -m64 icc -m64 -std=c11
`

**Benchmarks using Fortran, C, and C++:**
`
icpc -m64 icc -m64 -std=c11 ifort -m64
`

### Base Portability Flags

```
603.bwaves_s: -DSPEC_LP64
607.cactusBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
```

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Base Portability Flags (Continued)

627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs

Benmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

Benmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:

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Tested with SPEC CPU®2017 v1.0.5 on 2019-08-31 20:35:22-0400.
Originally published on 2019-09-19.