Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6252N, 2.30GHz)

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

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</tr>
<tr>
<td>548.exchange2_r 96</td>
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<td>239</td>
</tr>
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</table>

**Hardware**
- CPU Name: Intel Xeon Gold 6252N
- Max MHz: 3600
- Nominal: 2300
- Enabled: 48 cores, 2 chips, 2 threads/core
- Orderable: 1.2 Chips
- Cache L1: 32 KB I + 32 KB D on chip per core
- L2: 1 MB I+D on chip per core
- L3: 35.75 MB I+D on chip per chip
- Other: None
- Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
- Storage: 1 x 1.9 TB SSD SAS
- Other: None

**Software**
- OS: SUSE Linux Enterprise Server 15 (x86_64)
- Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- Parallel: No
- Firmware: Version 4.0.4c released Apr-2019
- File System: xfs
- System State: Run level 3 (multi-user)
- Base Pointers: 64-bit
- Peak Pointers: 32/64-bit
- Other: jemalloc memory allocator V5.0.1
- Power Management: --
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6252N, 2.30GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Results Table

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</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
  sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
  numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6252N, 2.30GHz)

SPECrater<sup>®</sup>2017<sub>int_base</sub> = 282
SPECrater<sup>®</sup>2017<sub>int_peak</sub> = 294

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

General Notes (Continued)
is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcede8f2999ca33d61f64985e4589ea9
running on linux-4z0x Sat Sep 14 12:43:52 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
- model name : Intel(R) Xeon(R) Gold 6252N CPU @ 2.30GHz
- 2 "physical id"s (chips)
- 96 "processors"
- cores, siblings (Caution: counting these is hw and system dependent. The following
  excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 24
  siblings : 48
  physical 0: cores 0 1 2 3 4 5 6 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29
  physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29

From lscpu:
- Architecture: x86_64
- CPU op-mode(s): 32-bit, 64-bit
- Byte Order: Little Endian
- CPU(s): 96
- On-line CPU(s) list: 0-95
- Thread(s) per core: 2
- Core(s) per socket: 24
- Socket(s): 2
- NUMA node(s): 4
- Vendor ID: GenuineIntel
- CPU family: 6
- Model: 85
- Model name: Intel(R) Xeon(R) Gold 6252N CPU @ 2.30GHz
- Stepping: 7

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6252N, 2.30GHz)

SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

SPECrate®2017_int_base = 282
SPECrate®2017_int_peak = 294

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Sep-2019
Hardware Availability: Apr-2019
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CPU MHz: 2300.000
CPU max MHz: 3600.0000
CPU min MHz: 1000.0000
BogoMIPS: 4600.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 36608K
NUMA node0 CPU(s): 0-3, 7, 8, 12-14, 18-20, 48-51, 55, 56, 60-62, 66-68
NUMA node1 CPU(s): 4-6, 9-11, 15-17, 21-23, 52-54, 57-59, 63-65, 69-71
NUMA node2 CPU(s): 24-27, 31-33, 37-39, 43, 44, 75-79, 81-87, 91, 92
NUMA node3 CPU(s): 28-30, 34-36, 40-42, 45-47, 76-78, 82-84, 88-90, 93-95
Flags: fpu vme de pse mce pae mtrr pge mca cmov
pat pse36 clflush dts acpica mxsr sse2 ss ht tm pbe syscall nx pdelgb dtscl
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_13 cdp_13 invpcid_single intel_ppip mba tpr_shadow vmi flexpriority ept
vpid fsqmstbase tsc_adjust bni hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsavec xsaves cmqm_llc cmqm_occup_llc cmqm_mbb_total cmqm_mbb_local
ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospke avx512_vnni arch_capabilities ssbd

/platform/cpuinfo cache data
  cache size: 36608 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 4 nodes (0-3)
nodes 0 cpus: 0 1 2 3 7 8 12 13 14 18 19 20 48 49 50 51 55 56 60 61 62 66 68
  node size: 192101 MB
  node free: 191557 MB
  node 1 cpus: 4 5 6 9 10 11 15 16 17 21 22 23 52 53 54 57 58 59 63 64 65 69 70 71
  node size: 193497 MB
  node free: 193182 MB
  node 2 cpus: 24 25 26 27 31 32 33 37 38 39 43 44 47 72 73 74 75 79 80 81 85 86 87 91 92
  node size: 193526 MB
  node free: 193274 MB
  node 3 cpus: 28 29 30 34 35 36 40 41 42 45 46 47 76 77 78 82 83 84 88 89 90 93 94 95
  node size: 193523 MB
  node free: 193272 MB
  node distances:
  node 0 1 2 3
  0: 10 11 21 21

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6252N, 2.30GHz)

SPECrate®2017_int_base = 282
SPECrate®2017_int_peak = 294

Platform Notes (Continued)

1:  11 10 21 21
2: 21 21 10 11
3: 21 21 11 10

From /proc/meminfo
   MemTotal:       791191776 kB
   HugePages_Total:       0
   Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
   os-release:
      NAME="SLES"
      VERSION="15"
      VERSION_ID="15"
      PRETTY_NAME="SUSE Linux Enterprise Server 15"
      ID="sles"
      ID_LIKE="suse"
      ANSI_COLOR="0;32"
      CPE_NAME="cpe:/o:suse:sles:15"

   uname -a:
      Linux linux-4z0x 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
         x86_64 x86_64 x86_64 GNU/Linux

   Kernel self-reported vulnerability status:

      CVE-2017-5754 (Meltdown): Not affected
      CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
      CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

   run-level 3 Sep 14 12:42

   SPEC is set to: /home/cpu2017
      Filesystem Type Size Used Avail Use% Mounted on
      /dev/sdaf1 xfs 891G 31G 860G 4% /

   Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
   BIOS Cisco Systems, Inc. C240M5.4.0.4c.0.0411190411 04/11/2019
   Memory:
      24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6252N, 2.30GHz)

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**Compiler Version Notes**

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Compiler Version Notes (Continued)

C++          |  523.xalancbmk_r(peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++          |  520.omnetpp_r(base, peak)  523.xalancbmk_r(base)
              |  531.deepsjeng_r(base, peak)  541.leela_r(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Fortran      |  548.exchange2_r(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
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Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64

(Continued on next page)
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Base Portability Flags (Continued)

502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

C++ benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m64 -std=c11


C++ benchmarks (except as noted below):
icpc -m64

523.xalancbmk_r: icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin

(Continued on next page)
## Cisco Systems
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### Peak Compiler Invocation (Continued)

Fortran benchmarks:

```plaintext
ifort -m64
```

### Peak Portability Flags

<table>
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<th>Benchmark</th>
<th>Flags</th>
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<tr>
<td>502.gcc_r</td>
<td>-D_FILE_OFFSET_BITS=64</td>
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<tr>
<td>505.mcf_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>520.omnia tp_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>-D_FILE_OFFSET_BITS=64 -DSPEC_LINUX</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>-DSPEC_LP64</td>
</tr>
</tbody>
</table>

### Peak Optimization Flags

C benchmarks:

```plaintext
500.perlb ench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4  
-fno-strict-overflow  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
-lqkmalloc
```

```plaintext
502.gcc_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4  
-L/usr/local/je5.0.1-32/lib -ljemalloc
```

```plaintext
505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
-lqkmalloc
```

```plaintext
525.x264_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4 -fno-alias  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
-lqkmalloc
```

```plaintext
557.xz_r: Same as 505.mcf_r
```

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6252N, 2.30GHz)

SPECrate®2017_int_base = 282
SPECrate®2017_int_peak = 294

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Sep-2019
Tested by: Cisco Systems
Hardware Availability: Apr-2019
Software Availability: May-2019

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