Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5215M, 2.50GHz)

SPECrater®2017_int_base = 119
SPECrater®2017_int_peak = Not Run

CPU2017 License: 9019
Test Date: Aug-2019
Test Sponsor: Cisco Systems
Hardware Availability: Apr-2019
Tested by: Cisco Systems
Software Availability: May-2019

Copies

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
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</tr>
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<tr>
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<tr>
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<tr>
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</tr>
<tr>
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<td>76.5</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>130</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>233</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>101</td>
</tr>
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</tr>
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<td>245</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>78.3</td>
</tr>
</tbody>
</table>

Hardware

CPU Name: Intel Xeon Gold 5215M
Max MHz: 3400
Nominal: 2500
Enabled: 20 cores, 2 chips, 2 threads/core
Orderable: 1.2 Chips
Cache L1: 32 KB I+ 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 13.75 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2666)
Storage: 1 x 960 GB SATA M.2 SSD
Other: None

Software

OS: SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
Parallel: No
Compiler: Version 4.0.4b released Apr-2019
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: None
Power Management: --
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Results Table

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<th>Benchmark</th>
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<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perfbench_r</td>
<td>40</td>
<td>701</td>
<td><strong>90.9</strong></td>
<td>705</td>
<td>90.4</td>
<td>698</td>
<td>91.2</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>40</td>
<td>595</td>
<td>95.2</td>
<td>600</td>
<td><strong>94.4</strong></td>
<td>600</td>
<td>94.3</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>40</td>
<td>412</td>
<td>157</td>
<td>414</td>
<td>156</td>
<td>413</td>
<td>157</td>
</tr>
<tr>
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<td>40</td>
<td>687</td>
<td>76.4</td>
<td>684</td>
<td>76.7</td>
<td><strong>686</strong></td>
<td><strong>76.5</strong></td>
</tr>
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<td>523.xalancbmk_r</td>
<td>40</td>
<td>325</td>
<td>130</td>
<td>326</td>
<td>130</td>
<td><strong>325</strong></td>
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</tr>
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<td>40</td>
<td>301</td>
<td>232</td>
<td>301</td>
<td>233</td>
<td>299</td>
<td>234</td>
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<td>40</td>
<td>456</td>
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<td>454</td>
<td>101</td>
</tr>
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<td>541.leela_r</td>
<td>40</td>
<td>714</td>
<td><strong>92.7</strong></td>
<td>712</td>
<td>93.0</td>
<td>716</td>
<td>92.5</td>
</tr>
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<td>40</td>
<td>427</td>
<td>245</td>
<td><strong>427</strong></td>
<td><strong>245</strong></td>
<td>428</td>
<td>245</td>
</tr>
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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
    sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
    numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)

(Continued on next page)
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General Notes (Continued)

is mitigated in the system as tested and documented.

Platform Notes

Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-3xnd Thu Sep  5 10:34:42 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 5215M CPU @ 2.50GHz
  2 "physical id"s (chips)
  40 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 10
siblings : 20
  physical 0: cores 0 1 2 3 4 8 9 10 11 12
  physical 1: cores 0 1 2 3 4 8 9 10 11 12

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 40
On-line CPU(s) list: 0-39
Thread(s) per core: 2
Core(s) per socket: 10
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 5215M CPU @ 2.50GHz
Stepping: 6
CPU MHz: 2500.000
CPU max MHz: 3400.0000
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Platform Notes (Continued)

CPU min MHz: 1000.0000
BogoMIPS: 5000.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 14080K
NUMA node0 CPU(s): 0-9,20-29
NUMA node1 CPU(s): 10-19,30-39
Flags: fpu vme de pse tsc msr pae mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpmr pdcm pclid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_i3 cdp_i3 invpcid_single intel_ppp mba tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust blkinhale avx2 smep bmi2 ertext cmp xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospe avx512_vnni arch_capabilities ssbd

/proc/cpuinfo cache data
  cache size : 14080 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 20 21 22 23 24 25 26 27 28 29
  node 0 size: 386560 MB
  node 0 free: 385836 MB
  node 1 cpus: 10 11 12 13 14 15 16 17 18 19 30 31 32 33 34 35 36 37 38 39
  node 1 size: 387015 MB
  node 1 free: 386569 MB
  node distances:

  node 0: 10 21
  node 1: 21 10

From /proc/meminfo
  MemTotal: 792142344 kB
  HugePages_Total: 0
  Hugepagesize: 4096 kB

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"

(Continued on next page)
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Platform Notes (Continued)

```bash
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"
```

```bash
uname -a:
Linux linux-3xnd 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux
run-level 3 Sep 5 10:14
```

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sdb4 xfs 100G 13G 88G 13% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2666

(End of data from sysinfo program)

Compiler Version Notes

```
C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base)
       | 525.x264_r(base) 557.xz_r(base)
-----------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----------------------------------------------

C++     | 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base)
       | 541.leela_r(base)
-----------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
```

(Continued on next page)
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Compiler Version Notes (Continued)

Fortran | 548.exchange2_r(base)
-----------------------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----------------------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

500.perlbach_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

(Continued on next page)
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Base Optimization Flags (Continued)

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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