Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6238M, 2.10GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Copies

<table>
<thead>
<tr>
<th>Test</th>
<th>Value</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perbench_r</td>
<td>88</td>
<td>190</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>88</td>
<td>198</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>88</td>
<td>315</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>88</td>
<td>165</td>
</tr>
<tr>
<td>523.xalanchmk_r</td>
<td>88</td>
<td>263</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>88</td>
<td>500</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>88</td>
<td>207</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>88</td>
<td>191</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>88</td>
<td>506</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>88</td>
<td>167</td>
</tr>
</tbody>
</table>

Hardware
CPU Name: Intel Xeon Gold 6238M
Max MHz: 3700
Nominal: 2100
Enabled: 44 cores, 2 chips, 2 threads/core
Orderable: 1,2 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 30.25 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
Storage: 1 x 240G SSD SATA
Other: None

Software
OS: SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
Parallel: No
Firmware: Version 4.0.4b released Apr-2019
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: None
Power Management: --
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6238M, 2.10GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>88</td>
<td>732</td>
<td>1918</td>
<td>737</td>
<td>1905</td>
<td>740</td>
<td>1895</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>88</td>
<td>629</td>
<td>198</td>
<td>628</td>
<td>198</td>
<td>627</td>
<td>199</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>88</td>
<td>451</td>
<td>315</td>
<td>450</td>
<td>316</td>
<td>453</td>
<td>314</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>88</td>
<td>701</td>
<td>165</td>
<td>699</td>
<td>165</td>
<td>700</td>
<td>165</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>88</td>
<td>354</td>
<td>263</td>
<td>353</td>
<td>263</td>
<td>353</td>
<td>262</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>525.x264_r</td>
<td>88</td>
<td>310</td>
<td>497</td>
<td>308</td>
<td>500</td>
<td>308</td>
<td>500</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>88</td>
<td>485</td>
<td>208</td>
<td>486</td>
<td>207</td>
<td>486</td>
<td>207</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>541.leela_r</td>
<td>88</td>
<td>762</td>
<td>191</td>
<td>754</td>
<td>193</td>
<td>762</td>
<td>191</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>88</td>
<td>455</td>
<td>507</td>
<td>456</td>
<td>505</td>
<td>456</td>
<td>506</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>557.xz_r</td>
<td>88</td>
<td>570</td>
<td>167</td>
<td>570</td>
<td>167</td>
<td>570</td>
<td>167</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

SPECrate®2017_int_base = 247
SPECrate®2017_int_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3 > /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
umactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6238M, 2.10GHz)

SPECrater®2017_int_base = 247
SPECrater®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

General Notes (Continued)

is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
- Intel HyperThreading Technology set to Enabled
- CPU performance set to Enterprise
- Power Performance Tuning set to OS Controls
- SNC set to Enabled
- IMC Interleaving set to 1-way Interleave
- Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-db10 Fri Sep 6 16:04:03 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Gold 6238M CPU @ 2.10GHz
  2 "physical id"s (chips)
  88 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 22
  siblings : 44
  physical 0: cores 0 1 2 3 4 5 8 9 10 11 12 16 17 18 19 20 21 24 25 26 27 28
  physical 1: cores 0 1 2 3 4 5 8 9 10 11 12 16 17 18 19 20 21 24 25 26 27 28

From lscpu:

Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 88
On-line CPU(s) list: 0-87
Thread(s) per core: 2
Core(s) per socket: 22
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6238M CPU @ 2.10GHz
Stepping: 7
CPU MHz: 2100.000

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6238M, 2.10GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECrater®2017_int_base = 247
SPECrater®2017_int_peak = Not Run

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

CPU max MHz: 3700.0000
CPU min MHz: 1000.0000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 30976K
NUMA node0 CPU(s): 0-2, 6-8, 11-13, 17, 18, 44-46, 50-52, 55-57, 61, 62
NUMA node1 CPU(s): 3-5, 9, 10, 14-16, 19-21, 47-49, 53, 54, 58-60, 63-65
NUMA node2 CPU(s): 22-24, 30-33, 35-39, 40, 66, 68, 72-74, 77-79, 83, 84
NUMA node3 CPU(s): 25-27, 31, 32, 36-38, 41-43, 49-51, 71, 75, 76, 80-82, 85-87
Flags: fpu vme de pse mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 stpmtd dca vmxvpt smep bmi1 bmi2 8vmx bmi2 epp bl segment HARDWARE: 1224

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6238M, 2.10GHz)

SPECrates®2017_int_base = 247
SPECrates®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Aug-2019
Tested by: Cisco Systems
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

2: 21 21 10 11
3: 21 21 11 10

From /proc/meminfo
MemTotal: 791003064 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-db10 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Sep 6 16:03

SPEC is set to: /home/cpu2017
filesystem type size used avail use% mounted on
/dev/sdc2 btrfs 222G 52G 170G 24% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6238M, 2.10GHz)  
SPECrade®2017_int_base = 247 
SPECrade®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Compiler Version Notes
==============================================================================
C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base)
       | 525.x264_r(base) 557.xz_r(base)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

C++     | 520.omnetpp_r(base) 523.xalanchbk_r(base) 531.deepsjeng_r(base)
       | 541.leela_r(base)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Fortran | 548.exchange2_r(base)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
  icc -m64 -std=c11

C++ benchmarks:
  icpc -m64

Fortran benchmarks:
  ifort -m64

Base Portability Flags
500.perlbench_r: -DSPEC_LP64  -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64

(Continued on next page)
Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6238M, 2.10GHz)  

| SPECrate®2017_int_base = 247 |
| SPECrate®2017_int_peak = Not Run |

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Aug-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

### Base Portability Flags (Continued)

523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX  
525.x264_r: -DSPEC_LP64  
531.deepsjeng_r: -DSPEC_LP64  
541.leela_r: -DSPEC_LP64  
548.exchange2_r: -DSPEC_LP64  
557.xz_r: -DSPEC_LP64

### Base Optimization Flags

**C benchmarks:**  
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
-lqkmalloc

**C++ benchmarks:**  
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
-lqkmalloc

**Fortran benchmarks:**  
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
-lqkmalloc

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:


### SPEC CPU and SPECrate

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.5 on 2019-09-06 19:04:02-0400.  
Originally published on 2019-10-01.