Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6222V, 1.80GHz)

SPECrater®2017_int_base = 201
SPECrater®2017_int_peak = 209

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Sep-2019
Tested by: Cisco Systems
Hardware Availability: Apr-2019
Software Availability: May-2019

<table>
<thead>
<tr>
<th>Software</th>
<th>Hardware</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS: SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default</td>
<td>CPU Name: Intel Xeon Gold 6222V</td>
</tr>
<tr>
<td>Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux</td>
<td>Max MHz: 3600</td>
</tr>
<tr>
<td>Firmware: Version 4.0.4g released Jul-2019</td>
<td>Nominal: 1800</td>
</tr>
<tr>
<td>System State: Run level 3 (multi-user)</td>
<td>Enabled: 40 cores, 2 chips, 2 threads/core</td>
</tr>
<tr>
<td>Base Pointers: 64-bit</td>
<td>Orderable: 1.2 Chips</td>
</tr>
<tr>
<td>Peak Pointers: 32/64-bit</td>
<td>Cache L1: 32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>Other: jemalloc memory allocator V5.0.1</td>
<td>L2: 1 MB I+D on chip per core</td>
</tr>
<tr>
<td>Power Management: --</td>
<td>L3: 27.5 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Other: None</td>
<td>Other: None</td>
</tr>
<tr>
<td>Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2400)</td>
<td>Storage: 1 x 1.9 TB SSD SAS</td>
</tr>
<tr>
<td>Other: None</td>
<td>Hardware</td>
</tr>
</tbody>
</table>
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6222V, 1.80GHz)

CPU2017 License: 9019  Test Sponsor: Cisco Systems  Tested by: Cisco Systems
Test Date: Sep-2019  Hardware Availability: Apr-2019  Software Availability: May-2019

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
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<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
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<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
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<td>176</td>
<td>726</td>
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<td>gcc_r</td>
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<td>670</td>
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<td>mcf_r</td>
<td>80</td>
<td>494</td>
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<td>138</td>
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<td>138</td>
<td>762</td>
<td>138</td>
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<tr>
<td>xalancbmk_r</td>
<td>80</td>
<td>384</td>
<td>220</td>
<td>382</td>
<td>221</td>
<td>381</td>
<td>222</td>
<td>80</td>
<td>358</td>
<td>236</td>
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<td>236</td>
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<td>x264_r</td>
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<td>deepsjeng_r</td>
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<td>164</td>
<td>559</td>
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<td>559</td>
<td>164</td>
</tr>
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<td>leela_r</td>
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<td>879</td>
<td>151</td>
<td>874</td>
<td>152</td>
<td>883</td>
<td>150</td>
<td>80</td>
<td>868</td>
<td>153</td>
<td>883</td>
<td>150</td>
<td>878</td>
<td>151</td>
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<tr>
<td>exchange2_r</td>
<td>80</td>
<td>533</td>
<td>394</td>
<td>531</td>
<td>394</td>
<td>531</td>
<td>394</td>
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<td>394</td>
<td>531</td>
<td>395</td>
<td>530</td>
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<td>xz_r</td>
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<td>136</td>
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<td>136</td>
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<td>636</td>
<td>136</td>
<td>636</td>
<td>136</td>
<td>635</td>
<td>136</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6222V, 1.80GHz)

SPEC CPU®2017 Integer Rate Result
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General Notes (Continued)

is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-cud8 Thu Sep 19 00:42:19 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6222V CPU @ 1.80GHz
  2 "physical id"s (chips)
  80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 20
siblings : 40
physical 0: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
physical 1: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 80
On-line CPU(s) list: 0-79
Thread(s) per core: 2
Core(s) per socket: 20
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6222V CPU @ 1.80GHz
Stepping: 7

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6222V, 1.80GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base = 201</th>
</tr>
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<tr>
<td>SPECrate®2017_int_peak = 209</td>
</tr>
</tbody>
</table>

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<th>CPU2017 License: 9019</th>
<th>Test Date:   Sep-2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>Hardware Availability: Apr-2019</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: May-2019</td>
</tr>
</tbody>
</table>

### Platform Notes (Continued)

- **CPU MHz:** 1800.000
- **CPU max MHz:** 3600.0000
- **CPU min MHz:** 800.0000
- **BogoMIPS:** 3600.00
- **Virtualization:** VT-x
- **L1d cache:** 32K
- **L1i cache:** 32K
- **L2 cache:** 1024K
- **L3 cache:** 28160K
- **NUMA node0 CPU(s):** 0-2,5,6,10-12,15,16,40-42,45,46,50-52,55,56
- **NUMA node1 CPU(s):** 3,4,7-9,13,14,17-19,43,44,47-49,53,54,57-59
- **NUMA node2 CPU(s):** 20-22,25,26,30-32,35,36,60-62,65,66,70-72,75,76
- **NUMA node3 CPU(s):** 23,24,27-29,33,34,37-39,63,64,67-69,73,74,77-79
- **Flags:** fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdelgb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xptr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_pراس mba tpr_shadow vnumi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ersed invpcid rtm cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsavec xsavec xsavec cmqm_llc cmqm_occup_llc cmqm_mbb_total cmqm_mbb_local ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni arch_capabilities ssbd

```
/platform/cpuinfo cache data
    cache size : 28160 KB
```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

<table>
<thead>
<tr>
<th>available: 4 nodes (0-3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>node 0 cpus: 0 1 2 5 6 10 11 12 15 16 40 41 42 45 46 50 51 52 55 56</td>
</tr>
<tr>
<td>node 0 size: 192103 MB</td>
</tr>
<tr>
<td>node 0 free: 191774 MB</td>
</tr>
<tr>
<td>node 1 cpus: 3 4 7 8 9 13 14 17 18 19 43 44 47 48 49 53 54 57 58 59</td>
</tr>
<tr>
<td>node 1 size: 193526 MB</td>
</tr>
<tr>
<td>node 1 free: 193267 MB</td>
</tr>
<tr>
<td>node 2 cpus: 20 21 22 25 26 30 31 32 35 36 60 61 62 65 66 70 71 72 75 76</td>
</tr>
<tr>
<td>node 2 size: 193526 MB</td>
</tr>
<tr>
<td>node 2 free: 193295 MB</td>
</tr>
<tr>
<td>node 3 cpus: 23 24 27 28 29 33 34 37 38 39 63 64 67 68 69 73 74 77 78 79</td>
</tr>
<tr>
<td>node 3 size: 193496 MB</td>
</tr>
<tr>
<td>node 3 free: 193089 MB</td>
</tr>
<tr>
<td>node distances:</td>
</tr>
<tr>
<td>node 0 1 2 3</td>
</tr>
<tr>
<td>0: 10 11 21 21</td>
</tr>
</tbody>
</table>

(Continued on next page)
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SPECrate®2017_int_base = 201
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Platform Notes (Continued)

1:  11 10 21 21
2:  21 21 10 11
3:  21 21 11 10

From /proc/meminfo
MemTotal:    791197084 kB
HugePages_Total:       0
Hugepagesize:    2048 kB

From /etc/*release* /etc/*version*
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-cud8 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Sep 19 00:36

SPEC is set to: /home/cpu2017

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C220M5.4.0.4g.0.0712190011 07/12/2019
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400

(End of data from sysinfo program)
Cisco Systems
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SPEC CPU®2017 Integer Rate Result
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Compiler Version Notes
==============================================================================
C       | 502.gcc_r(peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

C       | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
 | 525.x264_r(base, peak) 557.xz_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
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C       | 502.gcc_r(peak)
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C       | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
 | 525.x264_r(base, peak) 557.xz_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

C++     | 523.xalancbmk_r(peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

C++     | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
 | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,

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Compiler Version Notes (Continued)

Version 19.0.4.227 Build 20190416
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==============================================================================
C++ | 523.xalancbmk_r(peak)
==============================================================================
Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
C++ | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
C++ | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
==============================================================================
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
Fortran | 548.exchange2_r(base, peak)
==============================================================================
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64

(Continued on next page)
## Base Portability Flags (Continued)

- 502.gcc_r: -DSPEC_LP64
- 505.mcf_r: -DSPEC_LP64
- 520.omnetpp_r: -DSPEC_LP64
- 523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
- 525.x264_r: -DSPEC_LP64
- 531.deepsjeng_r: -DSPEC_LP64
- 541.leela_r: -DSPEC_LP64
- 548.exchange2_r: -DSPEC_LP64
- 557.xz_r: -DSPEC_LP64

## Base Optimization Flags

### C benchmarks:

- `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
- `-qopt-mem-layout-trans=4`
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64`
- `-lqkmalloc`

### C++ benchmarks:

- `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
- `-qopt-mem-layout-trans=4`
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64`
- `-lqkmalloc`

### Fortran benchmarks:

- `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
- `-qopt-mem-layout-trans=4`
- `-nostandard-realloc-lhs`
- `-align array32byte`
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64`
- `-lqkmalloc`

## Peak Compiler Invocation

### C benchmarks (except as noted below):

```bash
icc -m64 -std=c11
```


### C++ benchmarks (except as noted below):

```bash
icpc -m64
```

- 523.xalancbmk_r: `icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin`

---

(Continued on next page)
Peak Compiler Invocation (Continued)

Fortran benchmarks:
ifort -m64

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:

500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-fno-strict-overflow
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

502.gcc_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/jc5.0.1-32/lib -ljemalloc

505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

525.x264_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-alias
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

557.xz_r: Same as 505.mcf_r

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Peak Optimization Flags (Continued)

C++ benchmarks:

520.omnetpp_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

523.xalancbmk_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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