SPEC CPU®2017 Integer Rate Result

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Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL560 Gen10
(2.20 GHz, Intel Xeon Gold 5220)

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: Aug-2019

SPECrate®2017_int_base = 397
SPECrate®2017_int_peak = Not Run

<table>
<thead>
<tr>
<th>Copies</th>
<th>SPECrate®2017_int_base (397)</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r 144</td>
<td>305</td>
</tr>
<tr>
<td>502.gcc_r 144</td>
<td>319</td>
</tr>
<tr>
<td>505.mcf_r 144</td>
<td>536</td>
</tr>
<tr>
<td>520.omnetpp_r 144</td>
<td>273</td>
</tr>
<tr>
<td>523.xalancbmk_r 144</td>
<td>448</td>
</tr>
<tr>
<td>525.x264_r 144</td>
<td>813</td>
</tr>
<tr>
<td>531.deepsjeng_r 144</td>
<td>330</td>
</tr>
<tr>
<td>541.leela_r 144</td>
<td>307</td>
</tr>
<tr>
<td>548.exchange2_r 144</td>
<td>692</td>
</tr>
<tr>
<td>557.xz_r 144</td>
<td>268</td>
</tr>
</tbody>
</table>

Hardware

CPU Name: Intel Xeon Gold 5220
Max MHz: 3900
Nominal: 2200
Enabled: 72 cores, 4 chips, 2 threads/core
Orderable: 1, 2, 4 chip(s)
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 24.75 MB I+D on chip per chip
Other: None
Memory: 1536 GB (48 x 32 GB 2Rx4 PC4-2933Y-R, running at 2666)
Storage: 1 x 480 GB SAS SSD, RAID 0
Other: None

Software

OS: SUSE Linux Enterprise Server 15 (x86_64)
Compiler: C/C++: Version 19.0.2.187 of Intel C/C++ Compiler Build 20190117 for Linux;
Fortran: Version 19.0.2.187 of Intel Fortran Compiler Build 20190117 for Linux
Parallel: No
Firmware: HPE BIOS Version U34 02/02/2019 released Apr-2019
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: None
Power Management: --
Hewlett Packard Enterprise  
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<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>144</td>
<td>752</td>
<td>305</td>
<td>755</td>
<td>304</td>
<td>751</td>
<td>305</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>144</td>
<td>645</td>
<td>316</td>
<td>639</td>
<td>319</td>
<td>639</td>
<td>319</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>144</td>
<td>434</td>
<td>536</td>
<td>433</td>
<td>537</td>
<td>435</td>
<td>535</td>
</tr>
<tr>
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<td>144</td>
<td>692</td>
<td>273</td>
<td>691</td>
<td>274</td>
<td>692</td>
<td>273</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>144</td>
<td>340</td>
<td>536</td>
<td>339</td>
<td>449</td>
<td>339</td>
<td>448</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>144</td>
<td>309</td>
<td>817</td>
<td>310</td>
<td>813</td>
<td>311</td>
<td>810</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>144</td>
<td>500</td>
<td>330</td>
<td>500</td>
<td>330</td>
<td>500</td>
<td>330</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>144</td>
<td>778</td>
<td>307</td>
<td>787</td>
<td>303</td>
<td>776</td>
<td>307</td>
</tr>
<tr>
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<td>144</td>
<td>545</td>
<td>692</td>
<td>545</td>
<td>692</td>
<td>545</td>
<td>692</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>144</td>
<td>580</td>
<td>268</td>
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</tr>
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</table>

**Submit Notes**

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3 > /proc/sys/vm/drop_caches
```

runcpu command invoked through numactl i.e.:

```
umactl --interleave=all runcpu <etc>
```

**General Notes**

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH="/cpu2017/lib/ia32:/cpu2017/lib/intel64:/cpu2017/je5.0.1-32:/cpu2017/je5.0.1-64"
```

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM

memory using Redhat Enterprise Linux 7.5

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

(Continued on next page)
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Test Date: Sep-2019
Hardware Availability: Apr-2019
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General Notes (Continued)

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Configuration:
Thermal Configuration set to Maximum Cooling
Memory Patrol Scrubbing set to Disabled
LLC Prefetch set to Enabled
LLC Dead Line Allocation set to Disabled
Enhanced Processor Performance set to Enabled
Workload Profile set to General Throughput Compute
Workload Profile set to Custom
Energy/Performance Bias set to Balanced Performance
Advanced Memory Protection set to Advanced ECC
Sub-NUMA Clustering set to Disabled
Sysinfo program /cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on consip Fri Sep 20 08:51:58 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Gold 5220 CPU @ 2.20GHz
4 "physical id"s (chips)
144 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 18
siblings : 36
physical 0: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
physical 1: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
physical 2: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
physical 3: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 144
On-line CPU(s) list: 0-143
Thread(s) per core: 2

(Continued on next page)
Platform Notes (Continued)

Core(s) per socket:  18
Socket(s):           4
NUMA node(s):        4
Vendor ID:           GenuineIntel
CPU family:          6
Model:               85
Model name:          Intel(R) Xeon(R) Gold 5220 CPU @ 2.20GHz
Stepping:            6
CPU MHz:             2200.000
BogoMIPS:            4400.00
Virtualization:      VT-x
L1d cache:           32K
L1i cache:           32K
L2 cache:            1024K
L3 cache:            25344K
NUMA node0 CPU(s):   0-17,72-89
NUMA node1 CPU(s):   18-35,90-107
NUMA node2 CPU(s):   36-53,108-125
NUMA node3 CPU(s):   54-71,126-143
Flags:               fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
                      pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpentb
                      rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology
                      nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor
                      ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtrunc pdcm pcid dca
                     sse4_1 sse4_2 x2apic movbe popcnt
                      tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch
                      cpuid_fault ebp cat l3 cdpl cpuid_single intel_pmmu mbt tpr_shadow
                      vmx flexpriority ept
                      vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm
cqm mpx rdtd_a
                      avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd
                      avx512bw avx512vl
                      xsavesopt xsavec xgetbv1 xsaves cqm_llc cqm_occupt_llc cqm_mmb_total
                      cqm_mmb_local
                      ibpb ibrs stibp dtherm ida arat pln pts pku ospke avx512_vnni
                      arch_capabilities ssbd
                      /proc/cpuinfo cache data
cache size :  25344 KB

From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 4 nodes (0-3)
node 0 cpus:  0  1  2  3  4  5  6  7  8  9 10  11  12  13  14  15  16  17  18  19  20  21  22  23  24  25  26  27  28  29  30  31  32  33  34  35  36  37  38  39  40  41  42  43  44  45  46  47  48  49  50  51  52  53  54  55  56  57  58  59  60  61  62  63  64  65  66  67  68  69  70  71  72  73  74  75  76  77  78  79  80  81  82  83  84  85  86  87  88  89
node 0 size:  386549 MB
node 0 free:  386089 MB
node 1 cpus:  18  19  20  21  22  23  24  25  26  27  28  29  30  31  32  33  34  35  36  37  38  39  40  41  42  43  44  45  46  47  48  49  50  51  52  53  54  55  56  57  58  59  60  61  62  63  64  65  66  67  68  69  70  71  72  73  74  75  76  77  78  79  80  81  82  83  84  85  86  87  88  89
node 1 size:  387065 MB
node 1 free:  386767 MB
node 2 cpus:  54  55  56  57  58  59  60  61  62  63  64  65  66  67  68  69  70  71  72  73  74  75  76  77  78  79  80  81  82  83  84  85  86  87  88  89
node 2 size:  386089 MB
node 2 free:  387065 MB
(Continued on next page)
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Platform Notes (Continued)

node 2 size: 387065 MB
node 2 free: 386731 MB
node 3 cpus: 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 126 127 128 129 130 131 132 133 134 135 136 137 138 139 140 141 142 143
node 3 size: 386855 MB
node 3 free: 386469 MB
node distances:
node 0 1 2 3
0: 10 21 21 21
1: 21 10 21 21
2: 21 21 10 21
3: 21 21 21 10

From /proc/meminfo
MemTotal: 1584675760 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*

uname –a:
Linux consip 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b) x86_64
x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Sep 20 08:47

SPEC is set to: /cpu2017

Additional information from dmidecode follows. WARNING: Use caution when you interpret
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Platform Notes (Continued)

this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS HPE U34 02/02/2019
Memory:
48x UNKNOWN NOT AVAILABLE 32 GB 2 rank 2933, configured at 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base)
       | 525.x264_r(base) 557.xz_r(base)
==============================================================================
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.2.187 Build 20190117
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
C++     | 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base)
       | 541.leela_r(base)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.2.187 Build 20190117
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
Fortran | 548.exchange2_r(base)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.2.187 Build 20190117
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
  icc -m64 -std=c11

C++ benchmarks:
icpc -m64

(Continued on next page)
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SPECrates

<table>
<thead>
<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_base</td>
<td>397</td>
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### Base Compiler Invocation (Continued)

Fortran benchmarks:
ifort -m64

### Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

### Base Optimization Flags

C benchmarks:
-W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64
-lqkmalloc

C++ benchmarks:
-W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64
-lqkmalloc

The flags files that were used to format this result can be browsed at:
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.html
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You can also download the XML flags sources by saving the following links:

- [http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.xml](http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.xml)

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.5 on 2019-09-20 08:51:57-0400.  