SPEC CPU®2017 Integer Rate Result

Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8256, 3.80GHz)

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

<table>
<thead>
<tr>
<th>Copies</th>
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<tbody>
<tr>
<td>500.perlbench_r</td>
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<tr>
<td>502.gcc_r</td>
</tr>
<tr>
<td>505.mcf_r</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
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<tr>
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<td>525.x264_r</td>
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<tr>
<td>531.deepsjeng_r</td>
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</tr>
<tr>
<td>548.exchange2_r</td>
</tr>
<tr>
<td>557.xz_r</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Hardware</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name: Intel Xeon Platinum 8256</td>
</tr>
<tr>
<td>Max MHz: 3900</td>
</tr>
<tr>
<td>Nominal: 3800</td>
</tr>
<tr>
<td>Enabled: 8 cores, 2 chips, 2 threads/core</td>
</tr>
<tr>
<td>Orderable: 1 chip(s)</td>
</tr>
<tr>
<td>L1: 32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>L2: 16.5 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Other: None</td>
</tr>
<tr>
<td>Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)</td>
</tr>
<tr>
<td>Storage: 1 x 960 GB M.2 SATA SSD</td>
</tr>
<tr>
<td>Other: None</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Software</th>
</tr>
</thead>
<tbody>
<tr>
<td>Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux</td>
</tr>
<tr>
<td>Parallel: No</td>
</tr>
<tr>
<td>Firmware: Version 4.0.4b released Apr-2019</td>
</tr>
<tr>
<td>File System: btrfs</td>
</tr>
<tr>
<td>System State: Run level 3 (multi-user)</td>
</tr>
<tr>
<td>Base Pointers: 64-bit</td>
</tr>
<tr>
<td>Peak Pointers: Not Applicable</td>
</tr>
<tr>
<td>Other: None</td>
</tr>
<tr>
<td>Power Management: --</td>
</tr>
</tbody>
</table>
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8256, 3.80GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

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Results Table

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<thead>
<tr>
<th>Benchmark</th>
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</table>

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default

(Continued on next page)
## SPEC CPU®2017 Integer Rate Result

**Cisco Systems**

Cisco UCS B200 M5 (Intel Xeon Platinum 8256, 3.80GHz)

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<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
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<td>Cisco Systems</td>
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### General Notes (Continued)

- Prior to runcpu invocation
  - Filesystem page cache synced and cleared with:
    ```
sync; echo 3> /proc/sys/vm/drop_caches
    ```
  - runcpu command invoked through numactl i.e.:
    ```
    numactl --interleave=all runcpu <etc>
    ```

- **NA:** The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
- **Yes:** The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
- **Yes:** The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

### Platform Notes

- **BIOS Settings:**
  - Intel HyperThreading Technology set to Enabled
  - CPU performance set to Enterprise
  - Power Performance Tuning set to OS Controls
  - SNC set to Enabled
  - IMC interleave set to 1-way Interleave
  - Patrol Scrub set to Disabled

- **Sysinfo program /home/cpu2017/bin/sysinfo**
  - Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bccc091c0f
  - Viewing on: linux-5vrl Thu Sep 26 14:14:52 2019

- **SUT (System Under Test) info as seen by some common utilities.**
  - For more information on this section, see
    - [https://www.spec.org/cpu2017/Docs/config.html#sysinfo](https://www.spec.org/cpu2017/Docs/config.html#sysinfo)

- From /proc/cpuinfo
  ```
  model name : Intel(R) Xeon(R) Platinum 8256 CPU @ 3.80GHz
  2 "physical id"s (chips)
  16 "processors"
  cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 4
  siblings : 8
  ```

(Continued on next page)
### Platform Notes (Continued)

```
physical 0: cores 2 4 9 13
physical 1: cores 1 2 4 13

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 16
On-line CPU(s) list: 0-15
Thread(s) per core: 2
Core(s) per socket: 4
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Platinum 8256 CPU @ 3.80GHz
Stepping: 6
CPU MHz: 3800.000
CPU max MHz: 3900.0000
CPU min MHz: 1200.0000
BogoMIPS: 7600.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 16896K
NUMA node0 CPU(s): 0,2,8,10
NUMA node1 CPU(s): 1,3,9,11
NUMA node2 CPU(s): 4,5,12,13
NUMA node3 CPU(s): 6,7,14,15
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
```

### Non-Compliant

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Cisco Systems
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Platform Notes (Continued)

epb cat_l3 cpd_l3 invpcid_single interleave cpuid l3 tpr_shadow vnmi flexpriority ept
vpid fsgsbase tsc_adjust bmi1 hlt avx2 sm apic stkescl bmi2 erms invpcid rtm cqm
mpx rdtscp avx512vnni f16c rdrand vfmovq avx512bmi2 avx512bw avx512vl

/oproc/cpuinfo cache data
	cache size : 16896 KB
From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

available: 4 nodes (0-3)
node 0 cpus: 0 2 8 10
node 0 size: 192094 MB
node 0 free: 191845 MB
node 1 cpus: 1 3 9 11
node 1 size: 193524 MB
node 1 free: 193290 MB
node 2 cpus: 4 5 12 13
node 2 size: 193524 MB
node 2 free: 193297 MB
node 3 cpus: 6 7 14 15
node 3 size: 193493 MB
node 3 free: 193287 MB
node distances:
node 0 1 2 3
0: 10 11 21 21
1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10

From /proc/meminfo
	MemTotal:       791179972 kB
	HugePages_Total:       0
	Hugepagesize:       2048 kB

(Continued on next page)
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Platform Notes (Continued)

From /etc/*release* /etc/*version*

```bash
os-release:
  NAME="SLES"
  VERSION="15"
  VERSION_ID="15"
  PRETTY_NAME="SUSE Linux Enterprise Server 15"
  ID="sles"
  ID_LIKE="suse"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:15"
```

```bash
uname -a:
Linux linux-5vrl 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux
```

```bash
run-level 3 Sep 26 14:02
```

```bash
SPEC is set to /home/cpu2017
```

```bash
Filesystem Type Size Used Avail Use% Mounted on
/dev/sdb1 btrfs 224G 15G 208G 7% /home
```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow it to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019

Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base)
         | 525.x264_r(base) 557.xz_r(base)
==============================================================================

(Continued on next page)
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Compiler Version Notes (Continued)
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================
C++ | 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base)
| 541.leela_r(base)
==============================================================================
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================
Fortran | 548.exchange2_r(base)
==============================================================================
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================

Base Compiler Invocation
C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64
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Cisco UCS B200 M5 (Intel Xeon Platinum 8256, 3.80GHz)

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Base Portability Flags

500.perlbench_r -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r -DSPEC_LP64
505.mcf_r -DSPEC_LP64
520.omnetpp_r -DSPEC_LP64
523.xalancbmk_r -DSPEC_LP64 -DSPEC_LINUX
525.x264_r -DSPEC_LP64
531.deepsjeng_r -DSPEC_LP64
541.leela_r -DSPEC_LP64
548.exchange2_r -DSPEC_LP64
557.xz_r -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs, -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

C++ benchmarks:
-Wl,-z,muldefs, -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-Wl,-z,muldefs, -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8256, 3.80GHz) SPECrate®2017_int_base = SPECrate®2017_int_peak =

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The flags files that were used to format this result can be browsed at

You can also download the XML files sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-settings-V1.2-revJ.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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