SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.
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Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8256, 3.80GHz)

<table>
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<tbody>
<tr>
<td>9019</td>
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</tr>
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</table>

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Sep-2019

**Hardware Availability:** Apr-2019

**Software Availability:** May-2019

**CPU2017 License:** 9019

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**Test Date:** Sep-2019

**Hardware Availability:** Apr-2019

**Software Availability:** May-2019

**General Notes (Continued)**

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.


**Platform Notes**

**BIOS Settings:**
Intel HyperThreading Technology set to Disabled

CPU performance set to Enterprise

Power Performance Setting set to OS Controls

SNC set to Disabled

IMC Interleaving set to Auto

Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo

Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bce091c0f

running on Linux-5.10.14.r1 Sat Sep 28 11:51:21 2019

**SUT (System Under Test) info as seen by some common utilities.**

For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Platinum 8256 CPU @ 3.80GHz
            
   "physical id"s (chips) 8 "processors"
   cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

   cpu cores : 4
   siblings : 4
   physical 0: cores 2 4 9 13
   physical 1: cores 1 2 4 13
```

From lscpu:

(Continued on next page)
SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.
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Platform Notes (Continued)

/proc/cpuinfo cache data
  cache size : 16896 KB

From numactl --hardware
  WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3
  node 0 size: 385619 MB
  node 0 free: 381332 MB
  node 1 cpus: 4 5 6 7
  node 1 size: 387018 MB
  node 1 free: 386523 MB
  node distances:
    node   0   1
    0:   10  21
    1:   21  10

From /proc/meminfo
  MemTotal:       791181844 kB
  hugePages_Total:       0
  hugepagesize:       2048 kB

os-release: /etc/*release*/etc/*version*
  NAME="SLES"
  VERSION="15"
  VERSION_ID="15"
  RETRY_NAME="SUSE Linux Enterprise Server 15"
  ID="sles"
  ID_LIKE="suse"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
  Linux linux-5vrl 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
  x86_64 x86_64 x86_64 GNU/Linux

(Continued on next page)
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Platform Notes (Continued)

run-level 3 Sep 28 06:41
SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sdb1 btrfs 224G 18G 205G 8% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
 C       | 600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base)
 | 625.x264_s(base) 657.xz_s(base)
-------------------------------------------------------------------------------
 Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
 Version 19.0.4.227 Build 20190416
 Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-------------------------------------------------------------------------------

==============================================================================
 C++     | 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)
 | 641.xebla_s(base)
-------------------------------------------------------------------------------
 Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
 Version 19.0.4.227 Build 20190416
 Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

(Continued on next page)
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Compiler Version Notes (Continued)
==============================================================================
Fortran | 648.exchange2_s(base)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

639.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.fpp_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64
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Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPEOMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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