Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Platinum 8256, 3.80GHz)

SPECSpeed®2017_fp_base = 
SPECSpeed®2017_fp_peak =

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<table>
<thead>
<tr>
<th>Threads</th>
</tr>
</thead>
<tbody>
<tr>
<td>603.bwaves_s</td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
</tr>
<tr>
<td>619.lbm_s</td>
</tr>
<tr>
<td>621.wrf_s</td>
</tr>
<tr>
<td>627.cam4_s</td>
</tr>
<tr>
<td>628.pop2_s</td>
</tr>
<tr>
<td>638.imagick_s</td>
</tr>
<tr>
<td>644.nab_s</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
</tr>
<tr>
<td>654.roms_s</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Hardware</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name: Intel Xeon Platinum 8256</td>
</tr>
<tr>
<td>Max MHz: 3900</td>
</tr>
<tr>
<td>Nominal: 3800</td>
</tr>
<tr>
<td>Enabled: 8 cores, 2 chips</td>
</tr>
<tr>
<td>Orderable: 1,2 Chips</td>
</tr>
<tr>
<td>Cache L1: 32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>L2: 1 MB I+D on chip per core</td>
</tr>
<tr>
<td>L3: 16.5 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Other: None</td>
</tr>
<tr>
<td>Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)</td>
</tr>
<tr>
<td>Storage: 1 x 1.9 TB SSD SAS</td>
</tr>
<tr>
<td>Other: None</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Software</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS: SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default</td>
</tr>
<tr>
<td>Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux</td>
</tr>
<tr>
<td>Parallel: Yes</td>
</tr>
<tr>
<td>Firmware: Version 4.0.4g released Jul-2019</td>
</tr>
<tr>
<td>File System: xfs</td>
</tr>
<tr>
<td>System State: Run level 3 (multi-user)</td>
</tr>
<tr>
<td>Base Pointers: 64-bit</td>
</tr>
<tr>
<td>Peak Pointers: 64-bit</td>
</tr>
<tr>
<td>Other: None</td>
</tr>
<tr>
<td>Power Management: --</td>
</tr>
</tbody>
</table>

Test Date: Oct-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Test Sponsor: Cisco Systems
Tested by: Cisco Systems
CPU2017 License: 9019
Test Date: Oct-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Non-Compliant
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Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>603.bwaves_s</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
</tr>
<tr>
<td>619.lbm_s</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
</tr>
<tr>
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<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
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<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
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<td>NC</td>
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<td>NC</td>
<td>NC</td>
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<td>638.imagick_s</td>
<td>NC</td>
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<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
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<td>NC</td>
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<td>NC</td>
<td>NC</td>
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<td>NC</td>
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<td>NC</td>
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<td>NC</td>
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<tr>
<td>654.roms_s</td>
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<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
</tr>
</tbody>
</table>

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/old-cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
### General Notes (Continued)

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

### Platform Notes

BIOS Settings:
- Intel HyperThreading Technology set to Disabled
- CPU performance set to Enterprise
- Power Performance Tuning set to OS Controls
- SNC set to Disabled
- Patrol Scrub set to Disabled

Sysinfo program /home/old-cpu2017/bin/sysinfo

Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-diml Sun Oct  6 11:55:56 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
[https://www.spec.org/cpu2017/Docs/config.html#sysinfo](https://www.spec.org/cpu2017/Docs/config.html#sysinfo)

From /proc/cpuinfo
- model name : Intel(R) Xeon(R) Platinum 8256 CPU @ 3.80GHz
- 8 "physical id"s (chips)
  - 8 "processors"
- cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  - cpu cores : 4
  - siblings : 4
  - physical 0: cores 0 1 5 13
  - physical 1: cores 2 5 9 13

From lscpu:
- Architecture: x86_64
- CPU op-mode(s): 32-bit, 64-bit
- Byte Order: Little Endian
- CPU(s): 8

(Continued on next page)
Non-compliant

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SPEC CPU®2017 Floating Point Speed Result

Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Platinum 8256, 3.80GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base =</th>
<th>SPECspeed®2017_fp_peak =</th>
</tr>
</thead>
<tbody>
<tr>
<td>11.337</td>
<td>16.462</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Oct-2019
Hardware Availability: Apr-2019
Tested by: Cisco Systems
Software Availability: May-2019

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Platform Notes (Continued)

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3
node 0 size: 385635 MB
node 0 free: 378155 MB
node 1 cpus: 4 5 6 7
node 1 size: 387030 MB
node 1 free: 386557 MB
node distances:
node 0 1
0: 10 21
1: 21 10

From /proc/meminfo
MemTotal:       791210044 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-dim1 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected

(Continued on next page)
SPECFLOATING POINT SPEED RESULT

Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Platinum 8256, 3.80GHz)

| SPECspeed®2017_fp_peak = |
| SPECspeed®2017_fp_base = |

**CPU2017 License:** 9019  **Test Date:** Oct-2019  
**Test Sponsor:** Cisco Systems  **Hardware Availability:** Apr-2019  
**Tested by:** Cisco Systems  **Software Availability:** May-2019

SPECFLOATING POINT SPEED RESULT

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**Platform Notes (Continued)**

CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization  
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW  

run-level 3 Oct 6 06:59  

SPEC is set to: /home/old-cpu2017  
Filesistem Type  Size  Used Avail Use% Mounted on  
/dev/sda1 xfs  224G  44G  180G  20% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.  
BIOS Cisco Systems, Inc. C220M5.4.0.4g.0.0712190011 07/12/2019  
Memory:  
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934  

(End of data from sysinfo program)

**Compiler Version Notes**

C++  Fortran | 607.cactuBSSN_s(base, peak)

Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version: 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Non-Compliant
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Platinum 8256, 3.80GHz)

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Compiler Version Notes (Continued)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
Fortran         | 603.bwaves_s(base, peak) 649.fotonik3d_s(base, peak)
| 654.roms_s(base, peak)
------------------------------------------------------------------------------

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
Fortran, C      | 621.wrf_s(base, peak) 627.cam4_s(base, peak)
| 628.pop2_s(base, peak)
------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Platinum 8256, 3.80GHz)

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**Non-Compliant**

**Base Compiler Invocation (Continued)**

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

**Base Portability Flags**

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
71.roms_s: -DSPEC_LP64

**Base Optimization Flags**

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-
ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-
ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Platinum 8256, 3.80GHz) SPECspeed®2017 fp_base =
SPECspeed®2017 fp_peak =

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Base Optimization Flags (Continued)

Benchmarks using both Fortran and C:
-XCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

Benchmarks using Fortran, C, and C++:
-XCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11
Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags

Same as Base Portability Flags
SPEC CPU®2017 Floating Point Speed Result

Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Platinum 8256, 3.80GHz)

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<thead>
<tr>
<th>SPECspeed®2017_fp_base</th>
<th>SPECspeed®2017_fp_peak</th>
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Test Date: Oct-2019
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Software Availability: May-2019

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---

## Peak Optimization Flags

### C benchmarks:
- `-xCORE-AVX512` -ipo -03 -no-prec-div -qs -ope -refetch
- `-ffinite-math-only` -qopt-mem-layout-trans=4 -gopenmp -DSPEC_OPENMP

### Fortran benchmarks:
- `603.bwaves_s`: `-prof-gen(pass 1)` `-prof-use(pass 2)` `-DSPEC_SUPPRESS_OPENMP`
- `-DSPEC_OPENMP -02` `-xCORE-AVX512` `-qopt-trefetch -ipo -03`
- `-ffinite-math-only` -no-prec-div -qopt-mem-layout-trans=4
- `-gopenmp -nostandard-realloc-lhs`

- `649.fotonik3d_s`: Same as `603.bwaves_s`

- `654.roms_s`: `-DSPEC_OPENMP -xCORE-AVX512 -ipo -03 -no-prec-div`
- `-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4`
- `-gopenmp -nostandard-realloc-lhs`

### Benchmarks using Fortran and C:
- `621.wrf_s`: `-prof-gen(pass 1)` `-prof-use(pass 2) -02` `-xCORE-AVX512`
- `-qopt-prefetch -ipo -03 -ffinite-math-only -no-prec-div`
- `-qopt-mem-layout-trans=4 -DSPEC_SUPPRESS_OPENMP -gopenmp`
- `-DSPEC_OPENMP -nostandard-realloc-lhs`

- `624.num4_s`: `-xCORE-AVX512` `-ipo -03 -no-prec-div -qopt-prefetch`
- `-ffinite-math-only -qopt-mem-layout-trans=4` `-gopenmp`
- `-DSPEC_OPENMP -nostandard-realloc-lhs`

### Other benchmarks using Fortran, C, and C++:
- `-xCORE-AVX512` `-ipo -03 -no-prec-div -qopt-prefetch`
- `-ffinite-math-only` -qopt-mem-layout-trans=4 `-gopenmp` `-DSPEC_OPENMP`
- `-nostandard-realloc-lhs`
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Platinum 8256, 3.80GHz)

SPECspeed®2017_fp_base =
SPECspeed®2017_fp_peak =

CPU2017 License: 9019
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The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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