Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6240Y, 2.60GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECrate®2017_int_base = 225
SPECrate®2017_int_peak = 235

Test Date: Oct-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Hardware
CPU Name: Intel Xeon Gold 6240Y
Max MHz: 3900
Nominal: 2600
Enabled: 36 cores, 2 chips, 2 threads/core
Orderable: 1.2 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 24.75 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
Storage: 1 x 240 GB M.2 SATA SSD
Other: None

Software
OS: SUSE Linux Enterprise Server 15 (x86_64)
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
Parallel: No
Firmware: Version 4.0.4g released Jul-2019
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 32/64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: default
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Test Date: Oct-2019
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Results Table

<table>
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<td>557.xz_r</td>
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<td>147</td>
<td>72</td>
<td></td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.: (Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6240Y, 2.60GHz)

General Notes (Continued)

numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7ed1e6464a485a0011
running on linux-cud8 Thu Oct 24 20:50:41 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6240C CPU @ 2.60GHz
  2  "physical id"s (chips)
  72 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 18
siblings : 36
physical 0: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
physical 1: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27

From lscpu:
Architecture:          x86_64
CPU op-mode(s):        32-bit, 64-bit
Byte Order:            Little Endian
CPU(s):                72
On-line CPU(s) list:   0-71
Thread(s) per core:    2
Core(s) per socket:    18

(Continued on next page)
## Platform Notes (Continued)

<table>
<thead>
<tr>
<th>Socket(s):</th>
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<tbody>
<tr>
<td>NUMA node(s):</td>
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<tr>
<td>Vendor ID:</td>
<td>GenuineIntel</td>
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<tr>
<td>CPU family:</td>
<td>6</td>
</tr>
<tr>
<td>Model:</td>
<td>85</td>
</tr>
<tr>
<td>Model name:</td>
<td>Intel(R) Xeon(R) Gold 6240C CPU @ 2.60GHz</td>
</tr>
<tr>
<td>Stepping:</td>
<td>6</td>
</tr>
<tr>
<td>CPU MHz:</td>
<td>2600.000</td>
</tr>
<tr>
<td>CPU max MHz:</td>
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<td>L1d cache:</td>
<td>32K</td>
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<td>L1i cache:</td>
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<tr>
<td>L2 cache:</td>
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<td>L3 cache:</td>
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<td>NUMA node0 CPU(s):</td>
<td>0-2, 5, 6, 9, 10, 14, 15, 36-38, 41, 42, 45, 46, 50, 51</td>
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<tr>
<td>NUMA node1 CPU(s):</td>
<td>3, 4, 7, 8, 11-13, 16, 17, 39, 40, 43, 44, 47-49, 52, 53</td>
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<tr>
<td>NUMA node2 CPU(s):</td>
<td>18-20, 23, 24, 27, 28, 32, 33, 34-56, 59, 60, 63, 64, 68, 69</td>
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<td>NUMA node3 CPU(s):</td>
<td>21, 22, 25, 26, 29-31, 34, 35, 57, 58, 61, 62, 65-67, 70, 71</td>
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<tr>
<td>Flags:</td>
<td>fpu vme de pse tsc msr pae mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb reitwert nofxsr malleable</td>
</tr>
</tbody>
</table>
### Platform Notes (Continued)

node 2 free: 193312 MB  
node 3 cpus: 21 22 25 26 29 30 31 34 35 57 58 61 62 65 66 67 70 71  
node 3 size: 193496 MB  
node 3 free: 193286 MB  
node distances:  
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<th></th>
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</tr>
<tr>
<td>3</td>
<td>21</td>
<td>21</td>
<td>11</td>
<td>10</td>
</tr>
</tbody>
</table>

From /proc/meminfo  
MemTotal: 791198600 kB  
HugePages_Total: 0  
Hugepagesize: 2048 kB  

From /etc/*release* /etc/*version*  
```
NAME="SLES"  
VERSION="15"  
VERSION_ID="15"  
PRETTY_NAME="SUSE Linux Enterprise Server 15"  
ID="sles"  
ID_LIKE="suse"  
ANSI_COLOR="0;32"  
CPE_NAME="cpe:/o:suse:sles:15"
```

uname -a:  
```
Linux linux-cud8 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)  
x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:  

- CVE-2018-3620 (L1 Terminal Fault): No status reported  
- Microarchitectural Data Sampling: No status reported  
- CVE-2017-5754 (Meltdown): Not affected  
- CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp  
- CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization  
- CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW  

run-level 3 Oct 24 20:45

SPEC is set to: /home/cpu2017  
Filesystem Type Size Used Avail Use% Mounted on  
/dev/sda2 btrfs 224G 38G 186G 17% /home

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6240Y, 2.60GHz)

SPEC CPU®2017 Integer Rate Result

CPU2017 License: 9019
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Tested by: Cisco Systems

SPECrate®2017_int_base = 225
SPECrate®2017_int_peak = 235

Test Date: Oct-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

From /sys/devices/virtual/dmi/id
BIOS: Cisco Systems, Inc. C220M5.4.0.4g.0.0712190011 07/12/2019
Vendor: Cisco Systems Inc
Product: UCSC-C220-M5SX
Serial: WZP22380CRE

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)
The marketing name for the processor in this result, which appears in the CPU name and hardware model areas, is different from sysinfo because a pre-production processor was used. The pre-production processor differs from the production processor in name only.

Compiler Version Notes

==============================================================================
C       | 502.gcc_r(peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C       | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak) 525.x264_r(base, peak) 557.xz_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C       | 502.gcc_r(peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
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------------------------------------------------------------------------------

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Cisco Systems
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SPEC CPU®2017 Integer Rate Result

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Compiler Version Notes (Continued)

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<td>C</td>
<td>500.perlbench_r(base, peak)</td>
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<tr>
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<tr>
<td>C++</td>
<td>523.xalancbmk_r(peak)</td>
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<td>Fortran</td>
<td>548.exchange2_r(base, peak)</td>
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Compiler Version Notes (Continued)

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Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

(Continued on next page)
## Base Optimization Flags (Continued)

Fortran benchmarks:
- `-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
- `-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte`
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64`
- `-lqkmalloc`

## Peak Compiler Invocation

C benchmarks (except as noted below):
```
icc -m64 -std=c11
```

C++ benchmarks (except as noted below):
```
icpc -m64
```

Fortran benchmarks:
```
ifort -m64
```

## Peak Portability Flags

500.perlbench_r: `-DSPEC_LP64 -DSPEC_LINUX_X64`
502.gcc_r: `-D_FILE_OFFSET_BITS=64`
505.mcf_r: `-DSPEC_LP64`
520.omnetpp_r: `-DSPEC_LP64`
523.xalancbmk_r: `-D_FILE_OFFSET_BITS=64 -DSPEC_LINUX`
525.x264_r: `-DSPEC_LP64`
531.deepsjeng_r: `-DSPEC_LP64`
541.leela_r: `-DSPEC_LP64`
548.exchange2_r: `-DSPEC_LP64`
557.xz_r: `-DSPEC_LP64`

## Peak Optimization Flags

C benchmarks:
(Continued on next page)
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Peak Optimization Flags (Continued)

500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-fno-strict-overflow
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

502.gcc_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc

505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

525.x264_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-alias
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

557.xz_r: Same as 505.mcf_r

C++ benchmarks:

520.omnetpp_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

523.xalancbmk_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

SPEC CPU®2017 Integer Rate Result
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The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:


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