## CPU2017 Floating Point Rate Result

### Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Platinum 8260, 2.40GHz)

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<tr>
<th>SPECrate®2017_fp_base</th>
<th>SPECrate®2017_fp_peak</th>
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<tbody>
<tr>
<td>244</td>
<td>249</td>
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### Hardware

<table>
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<tr>
<th>Feature</th>
<th>Details</th>
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<tbody>
<tr>
<td>CPU Name</td>
<td>Intel Xeon Platinum 8260</td>
</tr>
<tr>
<td>Max MHz</td>
<td>3900</td>
</tr>
<tr>
<td>Nominal</td>
<td>2400</td>
</tr>
<tr>
<td>Enabled</td>
<td>48 cores, 2 chips, 2 threads/core</td>
</tr>
<tr>
<td>Orderable</td>
<td>1,2 Chips</td>
</tr>
<tr>
<td>Cache L1</td>
<td>32 KB I+ 32 KB D on chip per core</td>
</tr>
<tr>
<td>L2</td>
<td>1 MB I+D on chip per core</td>
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<tr>
<td>L3</td>
<td>35.75 MB I+D on chip per chip</td>
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<tr>
<td>Other</td>
<td>None</td>
</tr>
<tr>
<td>Memory</td>
<td>768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)</td>
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<tr>
<td>Storage</td>
<td>1 x 240 GB M.2 SATA SSD</td>
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<td>Other</td>
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### Software

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<td>SUSE Linux Enterprise Server 15 (x86_64)</td>
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<tr>
<td>Compiler</td>
<td>C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux</td>
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<tr>
<td>Parallel</td>
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<td>System State</td>
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<td>Base Pointers</td>
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<td>Peak Pointers</td>
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<td>Other</td>
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<td>Power Management</td>
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### Test Details

- **CPU2017 License:** 9019
- **Test Sponsor:** Cisco Systems
- **Tested by:** Cisco Systems
- **Hardware Availability:** Apr-2019
- **Software Availability:** May-2019
- **Test Date:** Oct-2019

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Standard Performance Evaluation Corporation (info@spec.org)  https://www.spec.org/
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Platinum 8260, 2.40GHz)

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</tbody>
</table>

SPECrate®2017_fp_base = 244
SPECrate®2017_fp_peak = 249

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Platinum 8260, 2.40GHz)

General Notes (Continued)

runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edbble6e46a485a0011

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Platinum 8260 CPU @ 2.40GHz
  2 "physical id"s (chips)
  96 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 24
siblings : 48
physical 0: cores 0 1 2 3 4 5 6 9 10 11 12 13 16 17 18 19 20 24 25 26 27 28 29
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 96
On-line CPU(s) list: 0-95
Thread(s) per core: 2
Core(s) per socket: 24
Socket(s): 2
NUMA node(s): 4

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Platinum 8260, 2.40GHz)

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
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<td>Test Sponsor:</td>
<td>Cisco Systems</td>
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<td>Cisco Systems</td>
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<td>Test Date:</td>
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<td>Apr-2019</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>May-2019</td>
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</tbody>
</table>

**SPEC CPU®2017 Floating Point Rate Result**

**SPECrate®2017_fp_base = 244**

**SPECrate®2017_fp_peak = 249**

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### Platform Notes (Continued)

Vendor ID:       GenuineIntel
CPU family:      6
Model:           85
Model name:      Intel(R) Xeon(R) Platinum 8260 CPU @ 2.40GHz
Stepping:        6
CPU MHz:         2400.000
CPU max MHz:     3900.0000
CPU min MHz:     1000.0000
BogoMIPS:        4800.00
Virtualization:  VT-x
L1d cache:       32K
L1i cache:       32K
L2 cache:        1024K
L3 cache:        36608K
NUMA node0 CPU(s): 0, 1, 2, 3, 7, 8, 12-14, 18-20, 48-51, 55, 56, 60-62, 66-68
NUMA node1 CPU(s): 4-6, 9-11, 15-17, 21-23, 52-54, 57-59, 63-65, 69-71
NUMA node2 CPU(s): 24-27, 31-33, 37-39, 43, 44, 72-75, 79-81, 85-87, 91, 92
NUMA node3 CPU(s): 28-30, 34-36, 40-42, 45-47, 76-78, 82-84, 88-90, 93-95
Flags:          fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
                 pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtsscp
                 lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
                 aperf perfctr tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
                 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
                 tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
                 epb cat_l3 cpdp_l3 invpcid_single intel_pinn mba tpr_shadow vmx flexpriority ept
                 vpid fsgsbase tsc_adjust bm11 hle avx2 smep bm12 erms invpd cmx rdt_a
                 avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
                 xsavesopt xsaveopt xgetbv1 xsaves cqm_llc cqm_occzip_llc cqm_mbb_total cqm_mbb_local
                 ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
                 ospke avx512_vnni arch_capabilities ssbd

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 7 8 12 13 14 18 19 20 48 49 50 51 55 56 60 61 62 66 67 68
node 0 size: 192101 MB
node 0 free: 178639 MB
node 1 cpus: 4 5 6 9 10 11 15 16 17 21 22 23 52 53 54 57 58 59 63 64 65 69 70 71
node 1 size: 193497 MB
node 1 free: 183493 MB
node 2 cpus: 24 25 26 27 31 32 33 37 38 39 43 44 72 73 74 75 79 80 81 85 86 87 91 92
node 2 size: 193526 MB
node 2 free: 183480 MB
node 3 cpus: 28 29 30 34 35 36 40 41 42 45 46 47 76 77 78 82 83 84 88 89 90 93 94 95

(Continued on next page)
Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Platinum 8260, 2.40GHz)

SPECrate®2017_fp_base = 244
SPECrate®2017_fp_peak = 249

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

node 3 size: 193523 MB
node 3 free: 183541 MB
node distances:
node 0 1 2 3
0: 10 11 21 21
1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10

From /proc/meminfo
MemTotal:       791191764 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*

NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-diml 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): No status reported
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Oct 23 13:53

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 xfs 224G 88G 136G 40% /

From /sys/devices/virtual/dmi/id

(Continued on next page)
Cisco Systems
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CPU2017 License: 9019
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Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

BIOS: Cisco Systems, Inc. C220M5.4.0.4g.0.0712190011 07/12/2019
Vendor: Cisco Systems Inc
Product: UCSC-C220-M5SX
Serial: WZP21310UGL

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

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<td>Copyright (C) 1985-2019 Intel Corporation. All rights reserved.</td>
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Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Platinum 8260, 2.40GHz)

SPECrate®2017_fp_base = 244
SPECrate®2017_fp_peak = 249

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Compiler Version Notes (Continued)

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

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Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Platinum 8260, 2.40GHz)

SPEC CPU®2017 Floating Point Rate Result
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Base Compiler Invocation (Continued)

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags
503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags
C benchmarks:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

C++ benchmarks:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

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Base Optimization Flags (Continued)

Benchmarks using both C and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags
Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
519.lbm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

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Peak Optimization Flags (Continued)

538.imagick_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

544.nab_r: Same as 538.imagick_r

C++ benchmarks:

508.namd_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

510.parest_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:

503.bwaves_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

549.fotonik3d_r: Same as 503.bwaves_r

554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both Fortran and C:

-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both C and C++:

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

526.blender_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch

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Peak Optimization Flags (Continued)

Benchmarks using Fortran, C, and C++ (continued):
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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