## SPEC CPU®2017 Integer Speed Result

### Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8276, 2.20GHz)

**SPECSpeed®2017_int_base = 7.79**  
**SPECSpeed®2017_int_peak = Not Run**

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</table>

### Hardware

- **CPU Name:** Intel Xeon Platinum 8276  
  - Max MHz: 4000  
  - Nominal: 2200  
  - Enabled: 112 cores, 4 chips  
  - Orderable: 2.4 Chips  
  - Cache L1: 32 KB I + 32 KB D on chip per core  
  - L2: 1 MB I+D on chip per core  
  - L3: 38.5 MB I+D on chip per chip  
  - Other: None  
  - Memory: 1536 GB (48 x 32 GB 2Rx4 PC4-2933V-R)  
  - Storage: 1 x 300 GB 15K RPM SAS HDD  
  - Other: None

### Software

- **OS:** SUSE Linux Enterprise Server 15 (x86_64)  
  - 4.12.14-23-default  
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;  
  - Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux  
- **Parallel:** Yes  
- **Firmware:** Version 4.0.3 released Mar-2019  
- **File System:** xfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** Not Applicable  
- **Other:** jemalloc memory allocator V5.0.1  
- **Power Management:** default
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8276, 2.20GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Oct-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Results Table

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</table>

SPECspeed®2017_int_base = 7.79
SPECspeed®2017_int_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
 sync; echo 3> /proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
## SPEC CPU®2017 Integer Speed Result

**Cisco Systems**

Cisco UCS C480 M5 (Intel Xeon Platinum 8276, 2.20GHz)

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<thead>
<tr>
<th>SPECspeed®2017_int_base</th>
<th>7.79</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed®2017_int_peak</td>
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</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Test Date:** Oct-2019  
**Tested by:** Cisco Systems  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

### Platform Notes

**BIOS Settings:**
- Intel HyperThreading Technology set to Disabled
- CPU performance set to Enterprise
- Power Performance Tuning set to OS Controls
- SNC set to Disabled
- Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r6365 of 2019-08-21 295195f888a3d7edeb16e6e46a485a0011  
running on linux-9yc8 Fri Oct 18 10:41:48 2019

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see  
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
- model name: Intel(R) Xeon(R) Platinum 8276 CPU @ 2.20GHz
  - 4 "physical id"s (chips)
  - 112 "processors"
- cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  - cpu cores: 28
  - siblings: 28
- physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30
- physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30
- physical 2: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30
- physical 3: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30

From lscpu:
- Architecture: x86_64
- CPU op-mode(s): 32-bit, 64-bit
- Byte Order: Little Endian
- CPU(s): 112
- On-line CPU(s) list: 0-111
- Thread(s) per core: 1
- Core(s) per socket: 28
- Socket(s): 4
- NUMA node(s): 4
- Vendor ID: GenuineIntel
- CPU family: 6
- Model: 85
- Model name: Intel(R) Xeon(R) Platinum 8276 CPU @ 2.20GHz
- Stepping: 7

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8276, 2.20GHz)

<table>
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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Oct-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

**Platform Notes (Continued)**

- **CPU MHz:** 2200.000
- **CPU max MHz:** 4000.0000
- **CPU min MHz:** 1000.0000
- **BogoMIPS:** 4400.00
- **Virtualization:** VT-x
- **L1d cache:** 32K
- **L1i cache:** 32K
- **L2 cache:** 1024K
- **L3 cache:** 39424K
- **NUMA node0 CPU(s):** 0-27
- **NUMA node1 CPU(s):** 28-55
- **NUMA node2 CPU(s):** 56-83
- **NUMA node3 CPU(s):** 84-111

**Flags:**
```
  fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperf perfctr tscKnownFreq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat L3 cdp L3 invpcid_single mba tpr_shadow vmmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mxp rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni arch_capabilities ssbd
```

**/proc/cpuinfo cache data**
```
cache size : 39424 KB
```

From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a physical chip.
```
  available: 4 nodes (0-3)  
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27  
  node 0 size: 385624 MB  
  node 0 free: 384611 MB  
  node 1 cpus: 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55  
  node 1 size: 387056 MB  
  node 1 free: 386533 MB  
  node 2 cpus: 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83  
  node 2 size: 387056 MB  
  node 2 free: 386834 MB  
  node 3 cpus: 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100 101 102 103 104 105 106 107 108 109 110 111  
  node 3 size: 387024 MB  
  node 3 free: 386790 MB
```
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8276, 2.20GHz)

<table>
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<tr>
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<th>9019</th>
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<td>Cisco Systems</td>
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<td>Tested by:</td>
<td>Cisco Systems</td>
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<td>Apr-2019</td>
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<tr>
<td>Software Availability:</td>
<td>May-2019</td>
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Platform Notes (Continued)

node distances:

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<td>1:</td>
<td>21</td>
<td>10</td>
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<td>21</td>
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<tr>
<td>3:</td>
<td>21</td>
<td>21</td>
<td>21</td>
<td>10</td>
</tr>
</tbody>
</table>

From /proc/meminfo

- MemTotal: 1583884132 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

From /etc/*release*/etc/*version*

- NAME="SLES"
- VERSION="15"
- VERSION_ID="15"
- PRETTY_NAME="SUSE Linux Enterprise Server 15"
- ID="sles"
- ID_LIKE="suse"
- ANSI_COLOR="0;32"
- CPE_NAME="cpe:/o:suse:sles:15"

uname -a:

```
Linux linux-9yc8 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

- CVE-2018-3620 (L1 Terminal Fault): No status reported
- Microarchitectural Data Sampling: No status reported
- CVE-2017-5754 (Meltdown): Not affected
- CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
- CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
- CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Oct 18 10:39

SPEC is set to: /home/cpu2017

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<tr>
<th>Filesystem</th>
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<th>Size</th>
<th>Used</th>
<th>Avail</th>
<th>Use%</th>
<th>Mounted on</th>
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<tr>
<td>/dev/sda1</td>
<td>xfs</td>
<td>280G</td>
<td>41G</td>
<td>239G</td>
<td>15%</td>
<td>/</td>
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From /sys/devices/virtual/dmi/id

- BIOS: Cisco Systems, Inc. C480M5.4.0.3.32.0301190121 03/01/2019
- Vendor: Cisco

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8276, 2.20GHz)

SPECspeed®2017_int_base = 7.79
SPECspeed®2017_int_peak = Not Run

Platform Notes (Continued)

Product: UCSC-C480-M5
Serial: FCH2238W00E

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
48x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

C
| 600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base) 625.x264_s(base) 657.xz_s(base)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++
| 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base) 641.leela_s(base)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Fortran
| 648.exchange2_s(base)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8276, 2.20GHz)

SPEC®2017 Integer Speed Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
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Base Compiler Invocation (Continued)

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -gopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8276, 2.20GHz)

SPECspeed®2017_int_base = 7.79
SPECspeed®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Oct-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.0 on 2019-10-18 13:41:47-0400.
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Software Availability: May-2019

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