Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6226, 2.70GHz)  

**SPECs**2017_fp_base = 163  
SPECs**2017_fp_peak = Not Run

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
<th>Test Date:</th>
<th>Oct-2019</th>
</tr>
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<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
<td>Hardware Availability:</td>
<td>Apr-2019</td>
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<td>Tested by:</td>
<td>Cisco Systems</td>
<td>Software Availability:</td>
<td>May-2019</td>
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</table>

### Hardware

<table>
<thead>
<tr>
<th>CPU Name:</th>
<th>Intel Xeon Gold 6226</th>
</tr>
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<tbody>
<tr>
<td>Max MHz:</td>
<td>3700</td>
</tr>
<tr>
<td>Nominal:</td>
<td>2700</td>
</tr>
<tr>
<td>Enabled:</td>
<td>48 cores, 4 chips</td>
</tr>
<tr>
<td>Orderable:</td>
<td>2,4 Chips</td>
</tr>
<tr>
<td>Cache L1:</td>
<td>32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>L2:</td>
<td>1 MB I+D on chip per core</td>
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<tr>
<td>L3:</td>
<td>19.25 MB I+D on chip per chip</td>
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<tr>
<td>Other:</td>
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<tr>
<td>Memory:</td>
<td>1536 GB (48 x 32 GB 2Rx4 PC4-2933V-R)</td>
</tr>
<tr>
<td>Storage:</td>
<td>1 x 300 GB 15K RPM SAS HDD</td>
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<tr>
<td>Other:</td>
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### Software

<table>
<thead>
<tr>
<th>OS:</th>
<th>SUSE Linux Enterprise Server 15 (x86_64)</th>
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<tr>
<td></td>
<td>4.12.14-23-default</td>
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<td>C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;</td>
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<tr>
<td>Fortran:</td>
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<td>Parallel:</td>
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<td>Firmware:</td>
<td>Version 4.0.3 released Mar-2019</td>
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<td>File System:</td>
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<tr>
<td>System State:</td>
<td>Run level 3 (multi-user)</td>
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<tr>
<td>Base Pointers:</td>
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<tr>
<td>Peak Pointers:</td>
<td>Not Applicable</td>
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<td>Other:</td>
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<td>Power Management:</td>
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SPEC CPU®2017 Floating Point Speed Result

Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6226, 2.70GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Results Table

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<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<tbody>
<tr>
<td>603.bwaves_s</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
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<td></td>
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<td>627.cam4_s</td>
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<td>649.fotonik3d_s</td>
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<td>82.9</td>
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<td>654.roms_s</td>
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<td>71.3</td>
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<td>71.8</td>
<td>219</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

SPECspeed®2017_fp_base = 163
SPECspeed®2017_fp_peak = Not Run

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6226, 2.70GHz)

| SPECspeed®2017_fp_base = 163 |
| SPECspeed®2017_fp_peak = Not Run |

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Oct-2019
Tested by: Cisco Systems
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f88a3d7eddb1e6e46a485a0011
running on linux-lozz Sun Oct 13 00:32:25 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
  model name : Intel(R) Xeon(R) Gold 6226 CPU @ 2.70GHz
  4 "physical id"s (chips)
  48 "processors"
  cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
    cpu cores : 12
    siblings : 12
    physical 0: cores 0 2 3 4 5 6 8 9 10 11 12 13
    physical 1: cores 0 2 3 4 5 6 8 9 10 11 13 14
    physical 2: cores 0 2 3 4 6 8 9 10 11 12 13 14
    physical 3: cores 0 2 3 5 6 8 9 10 11 12 13 14

From lscpu:
  Architecture: x86_64
  CPU op-mode(s): 32-bit, 64-bit
  Byte Order: Little Endian
  CPU(s): 48
  On-line CPU(s) list: 0-47
  Thread(s) per core: 1
  Core(s) per socket: 12
  Socket(s): 4
  NUMA node(s): 4
  Vendor ID: GenuineIntel
  CPU family: 6
  Model: 85
  Model name: Intel(R) Xeon(R) Gold 6226 CPU @ 2.70GHz
  Stepping: 7
  CPU MHz: 2700.000
  CPU max MHz: 3700.0000
  BogoMIPS: 5400.00

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6226, 2.70GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECspeed®2017_fp_base = 163
SPECspeed®2017_fp_peak = Not Run

Test Date: Oct-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

<table>
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<tr>
<th>Virtualization:</th>
<th>VT-x</th>
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<tbody>
<tr>
<td>L1d cache:</td>
<td>32K</td>
</tr>
<tr>
<td>L1i cache:</td>
<td>32K</td>
</tr>
<tr>
<td>L2 cache:</td>
<td>1024K</td>
</tr>
<tr>
<td>L3 cache:</td>
<td>19712K</td>
</tr>
<tr>
<td>NUMA node0 CPU(s):</td>
<td>0-11</td>
</tr>
<tr>
<td>NUMA node1 CPU(s):</td>
<td>12-23</td>
</tr>
<tr>
<td>NUMA node2 CPU(s):</td>
<td>24-35</td>
</tr>
<tr>
<td>NUMA node3 CPU(s):</td>
<td>36-47</td>
</tr>
</tbody>
</table>

Flags: 
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtsscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmperp tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdgb fma cx16 xptr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6226, 2.70GHz)

SPECSpeed®2017_fp_base = \hspace{1cm} 163
SPECSpeed®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

From /proc/meminfo
MemTotal: 1583896512 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15"
    VERSION_ID="15"
    PRETTY_NAME="SUSE Linux Enterprise Server 15"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
  Linux linux-lozz 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): No status reported
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Oct 12 22:07

SPEC is set to: /home/cpu2017
  Filesystem Type Size Used Avail Use% Mounted on
  /dev/sda2 xfs 273G 44G 229G 17% /

From /sys/devices/virtual/dmi/id
  BIOS: Cisco Systems, Inc. C480M5.4.0.3.32.0301190121 03/01/2019
  Vendor: Cisco
  Product: UCSC-C480-M5
  Serial: FCH2227W00H

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

(Continued on next page)
Platform Notes (Continued)

Memory:
48x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
<table>
<thead>
<tr>
<th>C</th>
<th>619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)</th>
</tr>
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</table>
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,   |
Version 19.0.4.227 Build 20190416                                         |
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.            |

==============================================================================
<table>
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<tr>
<th>C++, C, Fortran</th>
<th>607.cactuBSSN_s(base)</th>
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</thead>
</table>
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, |
Version 19.0.4.227 Build 20190416                                         |
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.            |

==============================================================================
<table>
<thead>
<tr>
<th>Fortran</th>
<th>603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)</th>
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</table>
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) |
64, Version 19.0.4.227 Build 20190416                                     |
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.            |

==============================================================================
<table>
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<tr>
<th>Fortran, C</th>
<th>621.wrf_s(base) 627.cam4_s(base) 628.pop2_s(base)</th>
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Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) |
64, Version 19.0.4.227 Build 20190416                                     |
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.            |

(Continued on next page)
## Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6226, 2.70GHz)

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<tr>
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<td>9019</td>
<td>163</td>
<td>Oct-2019</td>
<td>Apr-2019</td>
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<table>
<thead>
<tr>
<th>Test Sponsor</th>
<th>SPECspeed®2017_fp_peak</th>
<th>Tested by</th>
<th>Software Availability</th>
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<tbody>
<tr>
<td>Cisco Systems</td>
<td>Not Run</td>
<td>Cisco Systems</td>
<td>May-2019</td>
</tr>
</tbody>
</table>

### Compiler Version Notes (Continued)

#### Base Compiler Invocation

C benchmarks:
```
icc -m64 -std=c11
```

Fortran benchmarks:
```
ifort -m64
```

Benchmarks using both Fortran and C:
```
ifort -m64 icc -m64 -std=c11
```

Benchmarks using Fortran, C, and C++:
```
icpc -m64 icc -m64 -std=c11 ifort -m64
```

#### Base Portability Flags

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Flags</th>
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<tbody>
<tr>
<td>603.bwaves_s</td>
<td>-DSPEC_LP64</td>
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<tr>
<td>607.cactuBSSN_s</td>
<td>-DSPEC_LP64</td>
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<tr>
<td>619.lbm_s</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>621.wrf_s</td>
<td>-DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian</td>
</tr>
<tr>
<td>627.cam4_s</td>
<td>-DSPEC_LP64 -DSPEC_CASE_FLAG</td>
</tr>
<tr>
<td>628.pop2_s</td>
<td>-DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian -assume byte_recl</td>
</tr>
<tr>
<td>638.imagick_s</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>644.nab_s</td>
<td>-DSPEC_LP64</td>
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<td>649.fotonik3d_s</td>
<td>-DSPEC_LP64</td>
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<tr>
<td>654.roms_s</td>
<td>-DSPEC_LP64</td>
</tr>
</tbody>
</table>

#### Base Optimization Flags

C benchmarks:
```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
```

Fortran benchmarks:
```
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs
```

(Continued on next page)
## Base Optimization Flags (Continued)

Benchmarks using both Fortran and C:
- `xCORE-AVX512`  
- `-ipo`  
- `-O3`  
- `-no-prec-div`  
- `-qopt-prefetch`  
- `-ffinite-math-only`  
- `-qopt-mem-layout-trans=4`  
- `-qopenmp`  
- `-DSPEC_OPENMP`  
- `-nostandard-realloc-lhs`

Benchmarks using Fortran, C, and C++:
- `xCORE-AVX512`  
- `-ipo`  
- `-O3`  
- `-no-prec-div`  
- `-qopt-prefetch`  
- `-ffinite-math-only`  
- `-qopt-mem-layout-trans=4`  
- `-qopenmp`  
- `-DSPEC_OPENMP`  
- `-nostandard-realloc-lhs`

The flags files that were used to format this result can be browsed at:

You can also download the XML flags sources by saving the following links: