## SPEC CPU®2017 Integer Rate Result

**Tyrone Systems**  
(Test Sponsor: Netweb Pte Ltd)  
DS400TR-54/R  
(2.10 GHz, Intel Xeon Silver 4110)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>81.2</td>
<td>83.9</td>
</tr>
</tbody>
</table>

**Test Sponsor:** Netweb  
**Test Date:** Nov-2019  
**Hardware Availability:** Sep-2019  
**Software Availability:** Aug-2019

### Hardware

- **CPU Name:** Intel Xeon Silver 4110  
- **Max MHz:** 3000  
- **Nominal:** 2100  
- **Enabled:** 16 cores, 2 chips, 2 threads/core  
- **Orderable:** 1, 2 (chip)s  
- **Cache L1:** 32 KB I + 32 KB D on chip per core  
- **L2:** 1 MB I+D on chip per core  
- **L3:** 11 MB I+D on chip per chip  
- **Memory:** 384 GB (12 x 32 GB 2Rx4 PC4-2933P-R, running at 2400)  
- **Storage:** 1 x 480 GB SSD  
- **Other:** None

### Software

- **OS:** CentOS Linux release 7.7.1908 (Core) 3.10.0-1062.el7.x86_64  
- **Compiler:** C/C++: Version 19.0.4.243 of Intel C/C++ Compiler Build 20190416 for Linux; Fortran: Version 19.0.4.243 of Intel Fortran Compiler Build 20190416 for Linux  
- **Parallel:** No  
- **Firmware:** Version 3.1a released Jun-2019  
- **File System:** xfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** 32/64-bit  
- **Other:** jemalloc memory allocator V5.0.1  
- **Power Management:** None

---

### Copies

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>(81.2)</td>
<td>(83.9)</td>
</tr>
</tbody>
</table>

### Software

- **OS:** CentOS Linux release 7.7.1908 (Core) 3.10.0-1062.el7.x86_64  
- **Compiler:** C/C++: Version 19.0.4.243 of Intel C/C++ Compiler Build 20190416 for Linux; Fortran: Version 19.0.4.243 of Intel Fortran Compiler Build 20190416 for Linux  
- **Parallel:** No  
- **Firmware:** Version 3.1a released Jun-2019  
- **File System:** xfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** 32/64-bit  
- **Other:** jemalloc memory allocator V5.0.1  
- **Power Management:** None
**SPEC CPU® 2017 Integer Rate Result**

**Tyrone Systems**
(Test Sponsor: Netweb Pte Ltd)
DS400TR-54/R
(2.10 GHz, Intel Xeon Silver 4110)

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Base</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Peak</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>32</td>
<td>835</td>
<td>61.0</td>
<td>833</td>
<td>32</td>
<td>713</td>
<td>71.5</td>
<td>715</td>
<td>32</td>
<td>715</td>
<td>71.2</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>32</td>
<td>656</td>
<td>69.1</td>
<td>658</td>
<td>32</td>
<td>603</td>
<td>75.2</td>
<td>603</td>
<td>32</td>
<td>602</td>
<td>75.3</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>32</td>
<td>476</td>
<td>109</td>
<td>473</td>
<td>32</td>
<td>472</td>
<td>109</td>
<td>474</td>
<td>32</td>
<td>477</td>
<td>108</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>32</td>
<td>738</td>
<td>56.9</td>
<td>737</td>
<td>32</td>
<td>738</td>
<td>56.9</td>
<td>735</td>
<td>32</td>
<td>734</td>
<td>57.2</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>32</td>
<td>345</td>
<td>97.9</td>
<td>344</td>
<td>32</td>
<td>331</td>
<td>102</td>
<td>330</td>
<td>32</td>
<td>331</td>
<td>102</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>32</td>
<td>371</td>
<td>151</td>
<td>373</td>
<td>32</td>
<td>357</td>
<td>157</td>
<td>356</td>
<td>32</td>
<td>355</td>
<td>158</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>32</td>
<td>563</td>
<td>65.2</td>
<td>562</td>
<td>32</td>
<td>561</td>
<td>65.3</td>
<td>562</td>
<td>32</td>
<td>564</td>
<td>65.1</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>32</td>
<td>913</td>
<td>58.1</td>
<td>890</td>
<td>32</td>
<td>908</td>
<td>58.3</td>
<td>904</td>
<td>32</td>
<td>901</td>
<td>58.8</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>32</td>
<td>535</td>
<td>157</td>
<td>538</td>
<td>32</td>
<td>536</td>
<td>157</td>
<td>536</td>
<td>32</td>
<td>539</td>
<td>155</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>32</td>
<td>643</td>
<td>53.8</td>
<td>643</td>
<td>32</td>
<td>642</td>
<td>53.8</td>
<td>644</td>
<td>32</td>
<td>643</td>
<td>53.8</td>
</tr>
</tbody>
</table>

**Compiler Notes**

SPEC has learned that this result, which used an evaluation compiler, was submitted contrary to the compiler license terms.

Intel has granted a one-time waiver for this result.

**Submit Notes**

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.

For details, please see the config file.

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

**Environment Variables Notes**

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"
```
SPEC CPU®2017 Integer Rate Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)

DS400TR-54/R
(2.10 GHz, Intel Xeon Silver 4110)

SPECrate®2017_int_base = 81.2
SPECrate®2017_int_peak = 83.9

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Netweb

General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
  sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
  numactl --interleave=all runcpu <etc>
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edb1e6e46a485a0011
running on NODE3 Sat Nov 2 19:25:37 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
  https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
  model name : Intel(R) Xeon(R) Silver 4110 CPU @ 2.10GHz
  2 "physical id"s (chips)
  32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 8
  siblings : 16
  physical 0: cores 0 1 2 3 4 5 6 7
  physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:
  Architecture: x86_64
  CPU op-mode(s): 32-bit, 64-bit
  Byte Order: Little Endian
  CPU(s): 32
  On-line CPU(s) list: 0-31

(Continued on next page)
**SPEC CPU®2017 Integer Rate Result**

**Tyrone Systems**
(Test Sponsor: Netweb Pte Ltd)

**DS400TR-54/R**
(2.10 GHz, Intel Xeon Silver 4110)

---

**SPECrate®2017_int_base = 81.2**

**SPECrate®2017_int_peak = 83.9**

---

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>006042</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Netweb Pte Ltd</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Netweb</td>
</tr>
<tr>
<td>Test Date:</td>
<td>Nov-2019</td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Sep-2019</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Aug-2019</td>
</tr>
</tbody>
</table>

---

**Thread(s) per core:** 2  
**Core(s) per socket:** 8  
**Socket(s):** 2  
**NUMA node(s):** 2  
**Vendor ID:** GenuineIntel  
**CPU family:** 6  
**Model:** 85  
**Model name:** Intel(R) Xeon(R) Silver 4110 CPU @ 2.10GHz  
**Stepping:** 4  
**CPU MHz:** 800.061  
**CPU max MHz:** 3000.0000  
**CPU min MHz:** 800.0000  
**BogoMIPS:** 4200.00  
**Virtualization:** VT-x  
**L1d cache:** 32K  
**L1i cache:** 32K  
**L2 cache:** 1024K  
**L3 cache:** 11264K  
**NUMA node0 CPU(s):** 0-7,16-23  
**NUMA node1 CPU(s):** 8-15,24-31  
**Flags:** fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl apic reit_cbit lsu mmu_lsuPBS dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fmmul qdxt prtd cmc dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3nowprefetch eb xcpuid l1d intel_pipn intel_pt ssbd mba ibrs stibp tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsave xgetbv1 cqm_l1c cqm_occup_l1c cqm_mbm_total cqm_mbm_local dtherm ida arat pln pts pku ospke md_clear spec_ctrl intel_stibp flush_l1d

/proc/cpuinfo cache data  
**cache size:** 11264 KB

From numactl --hardware  
**WARNING:** a numactl 'node' might or might not correspond to a physical chip.  
**available:** 2 nodes (0-1)  
**node 0 cpus:** 0 1 2 3 4 5 6 7 16 17 18 19 20 21 22 23  
**node 0 size:** 195239 MB  
**node 0 free:** 190340 MB  
**node 1 cpus:** 8 9 10 11 12 13 14 15 24 25 26 27 28 29 30 31  
**node 1 size:** 196608 MB  
**node 1 free:** 192063 MB  
**node distances:**  
**node 0 1**  
**0: 10 21**

---

(Continued on next page)
**SPEC CPU®2017 Integer Rate Result**

**Tyrone Systems**
(Test Sponsor: Netweb Pte Ltd)
DS400TR-54/R
(2.10 GHz, Intel Xeon Silver 4110)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>81.2</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_peak</td>
<td>83.9</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 006042
**Test Sponsor:** Netweb Pte Ltd
**Tested by:** Netweb

<table>
<thead>
<tr>
<th>Test Date:</th>
<th>Nov-2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardware Availability:</td>
<td>Sep-2019</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Aug-2019</td>
</tr>
</tbody>
</table>

---

**Platform Notes (Continued)**

1: 21 10

From /proc/meminfo

MemTotal: 394875832 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release*/etc/*version*
centos-release: CentOS Linux release 7.7.1908 (Core)
centos-release-upstream: Derived from Red Hat Enterprise Linux 7.7 (Source)

From /sys/devices/virtual/dmi/id

BIOS: American Megatrends Inc. 3.1a 06/11/2019

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
DS400TR-54/R
(2.10 GHz, Intel Xeon Silver 4110)

SPECRate®2017_int_base = 81.2
SPECRate®2017_int_peak = 83.9

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Netweb

Platform Notes (Continued)

Vendor: Tyrone Systems
Product: X11DAi-N
Serial: 123456789

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
4x NO DIMM NO DIMM
12x Samsung M393A4K40CB2-CVF 32 GB 2 rank 2933

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C       | 502.gcc_r(peak)
==============================================================================
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.243 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
icc: NOTE: The evaluation period for this product ends on 2-nov-2019 UTC.
==============================================================================

==============================================================================
C       | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
        | 525.x264_r(base, peak) 557.xz_r(base, peak)
==============================================================================
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.243 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
icc: NOTE: The evaluation period for this product ends on 2-nov-2019 UTC.
==============================================================================

==============================================================================
C       | 502.gcc_r(peak)
==============================================================================
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.243 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
icc: NOTE: The evaluation period for this product ends on 2-nov-2019 UTC.
==============================================================================

==============================================================================
C       | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
==============================================================================
(Continued on next page)
SPEC CPU®2017 Integer Rate Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
DS400TR-54/R
(2.10 GHz, Intel Xeon Silver 4110)

SPECrates
SPECrates\textsuperscript{\textregistered}2017\textsubscript{\textregistered} int\textsubscript{\textsuperscript{\textregistered}} base = 81.2
SPECrates\textsuperscript{\textregistered}2017\textsubscript{\textregistered} int\textsubscript{\textsuperscript{\textregistered}} peak = 83.9

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Netweb

<table>
<thead>
<tr>
<th>CPU2017 License: 006042</th>
<th>Test Date: Nov-2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor: Netweb Pte Ltd</td>
<td>Hardware Availability: Sep-2019</td>
</tr>
<tr>
<td>Tested by: Netweb</td>
<td>Software Availability: Aug-2019</td>
</tr>
</tbody>
</table>

Compiler Version Notes (Continued)

<table>
<thead>
<tr>
<th>525.x264\textsubscript{r}(base, peak) 557.xz\textsubscript{r}(base, peak)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.243 Build 20190416</td>
</tr>
<tr>
<td>Copyright (C) 1985-2019 Intel Corporation. All rights reserved.</td>
</tr>
<tr>
<td>icc: NOTE: The evaluation period for this product ends on 2-nov-2019 UTC.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>523.xalancbmk\textsubscript{r}(peak)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.243 Build 20190416</td>
</tr>
<tr>
<td>Copyright (C) 1985-2019 Intel Corporation. All rights reserved.</td>
</tr>
<tr>
<td>icpc: NOTE: The evaluation period for this product ends on 2-nov-2019 UTC.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>520.omnetpp\textsubscript{r}(base, peak) 523.xalancbmk\textsubscript{r}(base)</th>
</tr>
</thead>
<tbody>
<tr>
<td>531.deepsjeng\textsubscript{r}(base, peak) 541.leela\textsubscript{r}(base, peak)</td>
</tr>
<tr>
<td>Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.243 Build 20190416</td>
</tr>
<tr>
<td>Copyright (C) 1985-2019 Intel Corporation. All rights reserved.</td>
</tr>
<tr>
<td>icpc: NOTE: The evaluation period for this product ends on 2-nov-2019 UTC.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>523.xalancbmk\textsubscript{r}(peak)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.243 Build 20190416</td>
</tr>
<tr>
<td>Copyright (C) 1985-2019 Intel Corporation. All rights reserved.</td>
</tr>
<tr>
<td>icpc: NOTE: The evaluation period for this product ends on 2-nov-2019 UTC.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>520.omnetpp\textsubscript{r}(base, peak) 523.xalancbmk\textsubscript{r}(base)</th>
</tr>
</thead>
<tbody>
<tr>
<td>531.deepsjeng\textsubscript{r}(base, peak) 541.leela\textsubscript{r}(base, peak)</td>
</tr>
<tr>
<td>Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.243 Build 20190416</td>
</tr>
<tr>
<td>Copyright (C) 1985-2019 Intel Corporation. All rights reserved.</td>
</tr>
<tr>
<td>icpc: NOTE: The evaluation period for this product ends on 2-nov-2019 UTC.</td>
</tr>
</tbody>
</table>

(Continued on next page)
**Tyrone Systems**  
(Test Sponsor: Netweb Pte Ltd)  
DS400TR-54/R  
(2.10 GHz, Intel Xeon Silver 4110)  

**SPEC CPU®2017 Integer Rate Result**  
Copyright 2017-2020 Standard Performance Evaluation Corporation  

| Test Date: | Nov-2019 |  
| Hardware Availability: | Sep-2019 |  
| Software Availability: | Aug-2019 |  

| CPU2017 License: | 006042 |  
| Test Sponsor: | Netweb Pte Ltd |  
| Tested by: | Netweb |  

**SPECrate®2017_int_base = 81.2**  
**SPECrate®2017_int_peak = 83.9**  

**Compiler Version Notes (Continued)**  
Fortran | 548.exchange2_r (base, peak)  
------------------------------------------------------------------------------  
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.0.4.243 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
ifort: NOTE: The evaluation period for this product ends on 2-nov-2019 UTC.  
------------------------------------------------------------------------------  

**Base Compiler Invocation**  
C benchmarks:  
icc -m64 -std=cl1  

C++ benchmarks:  
icpc -m64  

Fortran benchmarks:  
ifort -m64  

**Base Portability Flags**  
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64  
502.gcc_r: -DSPEC_LP64  
505.mcf_r: -DSPEC_LP64  
520.omnetpp_r: -DSPEC_LP64  
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX  
525.x264_r: -DSPEC_LP64  
531.deepsjeng_r: -DSPEC_LP64  
541.leela_r: -DSPEC_LP64  
548.exchange2_r: -DSPEC_LP64  
557.xz_r: -DSPEC_LP64  

**Base Optimization Flags**  
C benchmarks:  
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.243/linux/compiler/lib/intel64  
-lqkmalloc  

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
DS400TR-54/R
(2.10 GHz, Intel Xeon Silver 4110)

SPECrate®2017_int_base = 81.2
SPECrate®2017_int_peak = 83.9

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Netweb

Copyright 2017-2020 Standard Performance Evaluation Corporation

Base Optimization Flags (Continued)

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.243/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.243/linux/compiler/lib/intel64
-lqkmalloc

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m64 -std=c11


C++ benchmarks (except as noted below):
icpc -m64

523.xalancbmk_r: icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.243/linux/compiler/lib/ia32_lin

Fortran benchmarks:
ifort -m64

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64
SPEC CPU®2017 Integer Rate Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
DS400TR-54/R
(2.10 GHz, Intel Xeon Silver 4110)

SPECRate®2017_int_base = 81.2
SPECRate®2017_int_peak = 83.9

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Netweb

Test Date: Nov-2019
Hardware Availability: Sep-2019
Software Availability: Aug-2019

Peak Optimization Flags

C benchmarks:

500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -03 -no-prec-div -qopt-mem-layout-trans=4
-fno-strict-overflow
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.243/linux/compiler/lib/intel64
-lqkmalloc

502.gcc_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -03 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc

505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -03 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.243/linux/compiler/lib/intel64
-lqkmalloc

525.x264_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -03 -no-prec-div
-qopt-mem-layout-trans=4 -fno-alias
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.243/linux/compiler/lib/intel64
-lqkmalloc

557.xz_r: Same as 505.mcf_r

C++ benchmarks:

520.omnetpp_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -03 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.243/linux/compiler/lib/intel64
-lqkmalloc

523.xalancbmk_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -03 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -03 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.243/linux/compiler/lib/intel64
-lqkmalloc
<table>
<thead>
<tr>
<th>SPEC CPU®2017 Integer Rate Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Copyright 2017-2020 Standard Performance Evaluation Corporation</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Tyrone Systems</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Test Sponsor: Netweb Pte Ltd)</td>
</tr>
<tr>
<td>DS400TR-54/R</td>
</tr>
<tr>
<td>(2.10 GHz, Intel Xeon Silver 4110)</td>
</tr>
</tbody>
</table>

| SPECrate®2017_int_base = 81.2 |
| SPECrate®2017_int_peak = 83.9 |

<table>
<thead>
<tr>
<th>CPU2017 License: 006042</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor: Netweb Pte Ltd</td>
</tr>
<tr>
<td>Tested by: Netweb</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Test Date: Nov-2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardware Availability: Sep-2019</td>
</tr>
<tr>
<td>Software Availability: Aug-2019</td>
</tr>
</tbody>
</table>

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:


---

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.0 on 2019-11-02 09:55:36-0400.
Report generated on 2020-10-29 14:56:58 by CPU2017 PDF formatter v6255.