SPEC CPU®2017 Integer Rate Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
DS400TR-54/R/T
(2.80 GHz, Intel Xeon Gold 6242)

SPECrate®2017_int_base = 203
SPECrate®2017_int_peak = 211

Hardware

CPU Name: Intel Xeon Gold 6242
Max MHz: 3900
Nominal: 2800
Enabled: 32 cores, 2 chips, 2 threads/core
Orderable: 1, 2 (chip)s
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 22 MB I+D on chip per chip
Other: None
Memory: 384 GB (12 x 32 GB 2Rx4 PC4-2933P-R)
Storage: 1 x 480 GB SSD
Other: None

Software

OS: CentOS Linux release 7.7.1908 (Core)
3.10.0-1062.el7.x86_64
Compiler: C/C++: Version 19.0.4.243 of Intel C/C++
Compiler Build 20190416 for Linux;
Fortran: Version 19.0.4.243 of Intel Fortran
Compiler Build 20190416 for Linux
Parallel: No
Firmware: Version 3.1a released Jun-2019
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 32/64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: None

Copies

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base (203)</th>
<th>SPECrate®2017_int_peak (211)</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r 64</td>
<td></td>
</tr>
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<td></td>
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<td></td>
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<tr>
<td>557.xz_r 64</td>
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Test Date: Nov-2019
Hardware Availability: Sep-2019
Software Availability: Aug-2019
## SPEC CPU®2017 Integer Rate Result

### Results Table

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<thead>
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<th>Benchmark</th>
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<td><strong>130</strong></td>
</tr>
</tbody>
</table>

**SPECrate®2017_int_base = 203**

**SPECrate®2017_int_peak = 211**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Compiler Notes

SPEC has learned that this result, which used an evaluation compiler, was submitted contrary to the compiler license terms.

Intel has granted a one-time waiver for this result.

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.

For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH = 
    "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"
```

---

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SPEC✓CPU2017_int_peak = 211
SPEC✓CPU2017_int_base = 203

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General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7ed1e6e46a485a0011
running on NODE1 Tue Nov 5 02:54:42 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
  model name : Intel(R) Xeon(R) Gold 6242 CPU @ 2.80GHz
  2 "physical id"s (chips)
    64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
siblings : 32
  physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
  physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu:
  Architecture: x86_64
  CPU op-mode(s): 32-bit, 64-bit
  Byte Order: Little Endian
  CPU(s): 64
  On-line CPU(s) list: 0-63

(Continued on next page)
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SPEC CPU®2017 Integer Rate Result
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SPECrate®2017_int_base = 203  
SPECrate®2017_int_peak = 211

CPU2017 License: 006042  
Test Sponsor: Netweb Pte Ltd  
Tested by: Netweb

Test Date: Nov-2019  
Hardware Availability: Sep-2019  
Software Availability: Aug-2019

Thread(s) per core: 2  
Core(s) per socket: 16  
Socket(s): 2  
NUMA node(s): 2  
Vendor ID: GenuineIntel  
CPU family: 6  
Model: 85  
Model name: Intel(R) Xeon(R) Gold 6242 CPU @ 2.80GHz  
Stepping: 7  
CPU MHz: 1200.048  
CPU max MHz: 3900.0000  
CPU min MHz: 1200.0000  
BogoMIPS: 5600.00  
Virtualization: VT-x  
L1d cache: 32K  
L1i cache: 32K  
L2 cache: 1024K  
L3 cache: 22528K  
NUMA node0 CPU(s): 0-15,32-47  
NUMA node1 CPU(s): 16-31,48-63  
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc aperf perfctrperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtracompressed pdcmtsc市场需求 ts mtrrd rtprecedence ts_higher_priority aes xsave xsaveopt f16c rdrand lahf_lm abm 3nowprefetch ebpxe cat _l3 cdp _l3 intel_ppli intel_pros sbbd mba ibs ibp ibs _enhanced tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 0rms invpcid rtm cmq mxp rt aavx512f aavx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavesave xgetbv1 cqm_l1c cqm_occ1_l1c cqm_mbb1_total cqm_mbb1_local dtherm ida arat pts pkup ospe avx512_vnni md_clear spec_ctrl intel_stibp flush_lld arch_capabilities  

/platform/cpuinfo cacher data  
cache size : 22528 KB

From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a physical chip.  
available: 2 nodes (0-1)  
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47  
node 0 size: 195229 MB  
node 0 free: 190520 MB  
node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63  
node 1 size: 196608 MB  
node 1 free: 191570 MB  
node distances: 

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Test Date: Nov-2019
Hardware Availability: Sep-2019
Software Availability: Aug-2019

Platform Notes (Continued)

BIOS: American Megatrends Inc. 3.1a 06/11/2019
Vendor: Tyrone Systems
Product: X11DAi-N
Serial: 123456789

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
4x NO DIMM NO DIMM
12x Samsung M393A4K40CB2-CVF 32 GB 2 rank 2933

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C       | 502.gcc_r(peak)
==============================================================================
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.243 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
icc: NOTE: The evaluation period for this product ends on 2-nov-2019 UTC.

==============================================================================
C       | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak) 525.x264_r(base, peak) 557.xz_r(base, peak)
==============================================================================
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.243 Build 20190416
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(Continued on next page)
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**DS400TR-54/R/T**  
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**SPECrate®2017_int_peak = 211**

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**Compiler Version Notes (Continued)**

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**C**  
500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)  
525.x264_r(base, peak) 557.xz_r(base, peak)

---

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.243 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
icc: NOTE: The evaluation period for this product ends on 2-nov-2019 UTC.

---

**C++**  
523.xalancbmk_r(peak)

---

Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.243 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
icpc: NOTE: The evaluation period for this product ends on 2-nov-2019 UTC.

---

**C++**  
520.omnetpp_r(base, peak) 523.xalancbmk_r(base)  
531.deepsjeng_r(base, peak) 541.leela_r(base, peak)

---

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.243 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
icpc: NOTE: The evaluation period for this product ends on 2-nov-2019 UTC.

---

**C++**  
520.omnetpp_r(base, peak) 523.xalancbmk_r(base)  
531.deepsjeng_r(base, peak) 541.leela_r(base, peak)

---

Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.243 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
icpc: NOTE: The evaluation period for this product ends on 2-nov-2019 UTC.

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CPU2017 License: 006042  
Test Sponsor: Netweb Pte Ltd  
Tested by: Netweb  

Test Date: Nov-2019  
Hardware Availability: Sep-2019  
Software Availability: Aug-2019  

Compiler Version Notes (Continued)  

Fortran | 548.exchange2_r(base, peak)  
---------------------------------------------------------------------  
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.0.4.243 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
ifort: NOTE: The evaluation period for this product ends on 2-nov-2019 UTC.

Base Compiler Invocation  

C benchmarks:  
icc -m64 -std=c11  

C++ benchmarks:  
icpc -m64  

Fortran benchmarks:  
ifort -m64  

Base Portability Flags  

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64  
502.gcc_r: -DSPEC_LP64  
505.mcf_r: -DSPEC_LP64  
520.omnetpp_r: -DSPEC_LP64  
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX  
525.x264_r: -DSPEC_LP64  
531.deepsjeng_r: -DSPEC_LP64  
541.leela_r: -DSPEC_LP64  
548.exchange2_r: -DSPEC_LP64  
557.xz_r: -DSPEC_LP64  

Base Optimization Flags  

C benchmarks:  
-W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.243/linux/compiler/lib/intel64  
-lqkmalloc
Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
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Test Date: Nov-2019
Hardware Availability: Sep-2019
Software Availability: Aug-2019

Base Optimization Flags (Continued)

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.243/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.243/linux/compiler/lib/intel64
-lqkmalloc

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m64 -std=c11


C++ benchmarks (except as noted below):
icpc -m64

523.xalancbmk_r: icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.243/linux/compiler/lib/ia32_lin

Fortran benchmarks:
ifort -m64

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64
## Peak Optimization Flags

### C benchmarks:

500.perlbench_r: -Wl, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -03 -no-prec-div -qopt-mem-layout-trans=4  
-fno-strict-overflow  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.243/linux/compiler/lib/intel64  
-lqkmalloc

502.gcc_r: -Wl, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -03 -no-prec-div -qopt-mem-layout-trans=4  
-L/usr/local/jemalloc  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.243/linux/compiler/lib/intel64  
-lqkmalloc

505.mcf_r: -Wl, -z, muldefs -xCORE-AVX512 -ipo -03 -no-prec-div  
-qopt-mem-layout-trans=4  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.243/linux/compiler/lib/intel64  
-lqkmalloc

525.x264_r: -Wl, -z, muldefs -xCORE-AVX512 -ipo -03 -no-prec-div  
-qopt-mem-layout-trans=4 -fno-alias  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.243/linux/compiler/lib/intel64  
-lqkmalloc

557.xz_r: Same as 505.mcf_r

### C++ benchmarks:

520.omnetpp_r: -Wl, -z, muldefs -xCORE-AVX512 -ipo -03 -no-prec-div  
-qopt-mem-layout-trans=4  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.243/linux/compiler/lib/intel64  
-lqkmalloc

523.xalancbmk_r: -Wl, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -03 -no-prec-div -qopt-mem-layout-trans=4  
-L/usr/local/jemalloc  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.243/linux/compiler/lib/intel64  
-lqkmalloc

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

### Fortran benchmarks:

-Wl, -z, muldefs -xCORE-AVX512 -ipo -03 -no-prec-div  
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.243/linux/compiler/lib/intel64  
-lqkmalloc
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Test Date: Nov-2019
Hardware Availability: Sep-2019
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The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.0 on 2019-11-05 02:54:41-0500.