SPEC CPU®2017 Floating Point Rate Result

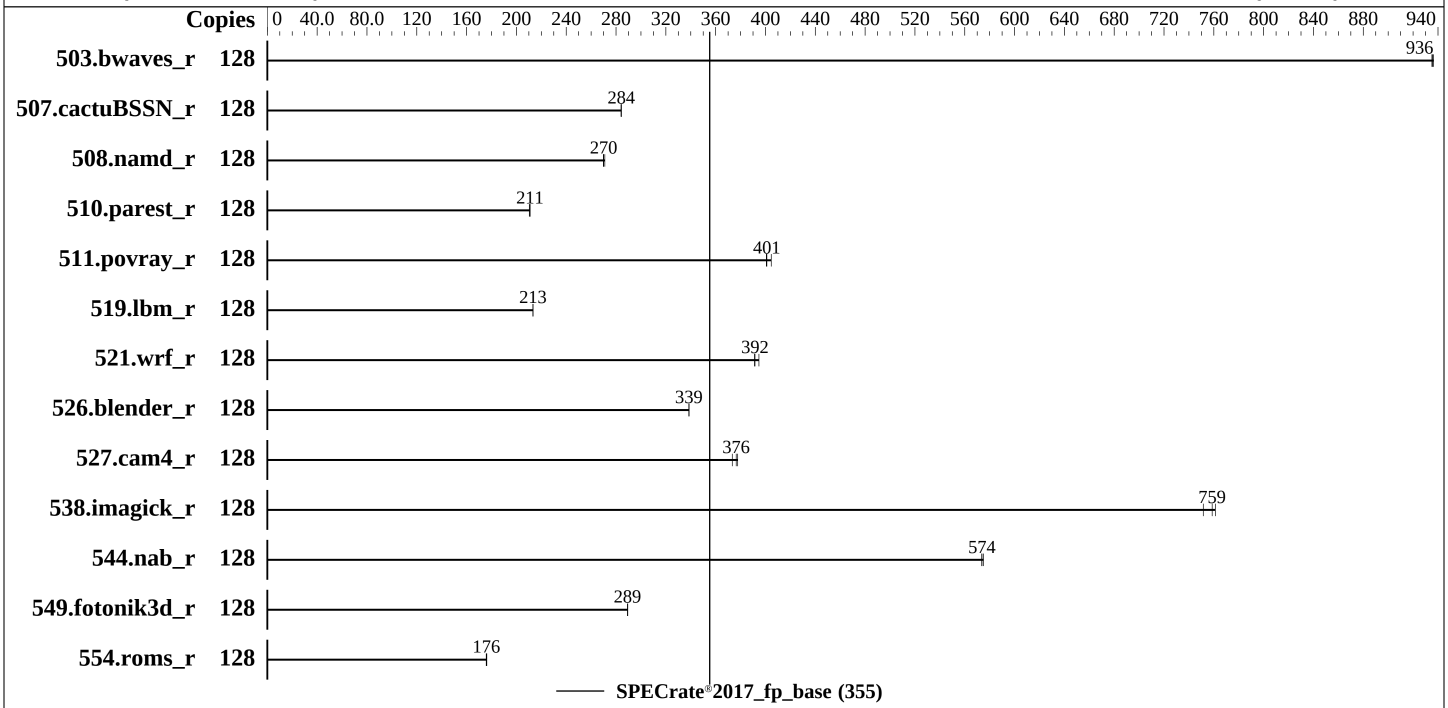
Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 5218, 2.30GHz)

SPECrate®2017_fp_base = 355

SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Nov-2019
Hardware Availability: Apr-2019
Software Availability: May-2019



Hardware

CPU Name: Intel Xeon Gold 5218
Max MHz: 3900
Nominal: 2300
Enabled: 64 cores, 4 chips, 2 threads/core
Orderable: 2,4 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 22 MB I+D on chip per chip
Other: None
Memory: 1536 GB (48 x 32 GB 2Rx4 PC4-2933V-R, running at 2666)
Storage: 1 x 1.9 TB SSD SAS
Other: None

Software

OS: SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-25.28-default
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
Parallel: No
Firmware: Version 4.0.4g released Jul-2019
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: None
Power Management: default

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Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
503.bwaves_r	128	**1372**	**936**	1373	935	1371	936							
507.cactuBSSN_r	128	570	284	**570**	**284**	571	284							
508.namd_r	128	451	270	449	271	**450**	**270**							
510.parest_r	128	**1587**	**211**	1587	211	1592	210							
511.povray_r	128	**745**	**401**	746	401	739	405							
519.lbm_r	128	632	213	633	213	**632**	**213**							
521.wrf_r	128	726	395	**732**	**392**	733	391							
526.blender_r	128	576	339	**576**	**339**	576	338							
527.cam4_r	128	**595**	**376**	600	373	593	378							
538.imagick_r	128	**420**	**759**	418	761	424	752							
544.nab_r	128	**375**	**574**	375	575	376	574							
549.fotonik3d_r	128	1725	289	1723	289	**1725**	**289**							
554.roms_r	128	**1156**	**176**	1154	176	1157	176							

SPECrate®2017_fp_base = 355

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

```
The numactl mechanism was used to bind copies to processors. The config file option 'submit'
was used to generate numactl commands to bind each copy to a specific processor.
For details, please see the config file.
```

Operating System Notes

```
Stack size set to unlimited using "ulimit -s unlimited"
```

Environment Variables Notes

```
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
```

General Notes

```
Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>       /proc/sys/vm/drop_caches
```

(Continued on next page)

General Notes (Continued)

```
 runcpu command invoked through numactl i.e.:
 numactl --interleave=all runcpu &lt;etc&gt;
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
```

Platform Notes

```
BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled

 Sysinfo program /home/cpu2017/bin/sysinfo
 Rev: r6365 of 2019-08-21 295195f888a3d7edb1e6e46a485a0011
 running on linux-75co Wed Nov  6 12:36:45 2019

 SUT (System Under Test) info as seen by some common utilities.
 For more information on this section, see
    https://www.spec.org/cpu2017/Docs/config.html#sysinfo

 From /proc/cpuinfo
    model name : Intel(R) Xeon(R) Gold 5218 CPU @ 2.30GHz
       4  "physical id"s (chips)
       128 "processors"
    cores, siblings (Caution: counting these is hw and system dependent. The following
    excerpts from /proc/cpuinfo might not be reliable.  Use with caution.)
       cpu cores : 16
       siblings  : 32
       physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
       physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
       physical 2: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
       physical 3: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

 From lscpu:
      Architecture:        x86_64
      CPU op-mode(s):      32-bit, 64-bit
      Byte Order:          Little Endian
      CPU(s):              128
      On-line CPU(s) list: 0-127
      Thread(s) per core:  2
      Core(s) per socket:  16
```

(Continued on next page)

Platform Notes (Continued)

```
     Socket(s):             4
     NUMA node(s):          8
     Vendor ID:             GenuineIntel
     CPU family:            6
     Model:                 85
     Model name:            Intel(R) Xeon(R) Gold 5218 CPU @ 2.30GHz
     Stepping:              6
     CPU MHz:               2300.000
     CPU max MHz:           3900.0000
     CPU min MHz:           1000.0000
     BogoMIPS:              4600.00
     Virtualization:        VT-x
     L1d cache:             32K
     L1i cache:             32K
     L2 cache:              1024K
     L3 cache:              22528K
     NUMA node0 CPU(s):     0-3,8-11,64-67,72-75
     NUMA node1 CPU(s):     4-7,12-15,68-71,76-79
     NUMA node2 CPU(s):     16-19,24-27,80-83,88-91
     NUMA node3 CPU(s):     20-23,28-31,84-87,92-95
     NUMA node4 CPU(s):     32-35,40-43,96-99,104-107
     NUMA node5 CPU(s):     36-39,44-47,100-103,108-111
     NUMA node6 CPU(s):     48-51,56-59,112-115,120-123
     NUMA node7 CPU(s):     52-55,60-63,116-119,124-127
     Flags:                 fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
     pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
     lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
     aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
     xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
     avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3
     invpcid_single intel_ppin ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi
     flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm
     cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd
     avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total
     cqm_mbm_local dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
     ospke avx512_vnni flush_l1d arch_capabilities

 /proc/cpuinfo cache data
    cache size : 22528 KB

 From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a
 physical chip.
   available: 8 nodes (0-7)
   node 0 cpus: 0 1 2 3 8 9 10 11 64 65 66 67 72 73 74 75
   node 0 size: 192101 MB
   node 0 free: 186768 MB
   node 1 cpus: 4 5 6 7 12 13 14 15 68 69 70 71 76 77 78 79
```

(Continued on next page)

Platform Notes (Continued)

```
    node 1 size: 193503 MB
    node 1 free: 189796 MB
    node 2 cpus: 16 17 18 19 24 25 26 27 80 81 82 83 88 89 90 91
    node 2 size: 193532 MB
    node 2 free: 190064 MB
    node 3 cpus: 20 21 22 23 28 29 30 31 84 85 86 87 92 93 94 95
    node 3 size: 193532 MB
    node 3 free: 190063 MB
    node 4 cpus: 32 33 34 35 40 41 42 43 96 97 98 99 104 105 106 107
    node 4 size: 193532 MB
    node 4 free: 190047 MB
    node 5 cpus: 36 37 38 39 44 45 46 47 100 101 102 103 108 109 110 111
    node 5 size: 193532 MB
    node 5 free: 190069 MB
    node 6 cpus: 48 49 50 51 56 57 58 59 112 113 114 115 120 121 122 123
    node 6 size: 193532 MB
    node 6 free: 190028 MB
    node 7 cpus: 52 53 54 55 60 61 62 63 116 117 118 119 124 125 126 127
    node 7 size: 193531 MB
    node 7 free: 190063 MB
    node distances:
    node   0   1   2   3   4   5   6   7
      0:  10  11  21  21  21  21  31  31
      1:  11  10  21  21  21  21  31  31
      2:  21  21  10  11  31  31  21  21
      3:  21  21  11  10  31  31  21  21
      4:  21  21  31  31  10  11  21  21
      5:  21  21  31  31  11  10  21  21
      6:  31  31  21  21  21  21  10  11
      7:  31  31  21  21  21  21  11  10

  From /proc/meminfo
     MemTotal:       1583923264 kB
     HugePages_Total:       0
     Hugepagesize:       2048 kB

  From /etc/*release* /etc/*version*
     os-release:
        NAME="SLES"
        VERSION="15"
        VERSION_ID="15"
        PRETTY_NAME="SUSE Linux Enterprise Server 15"
        ID="sles"
        ID_LIKE="suse"
        ANSI_COLOR="0;32"
        CPE_NAME="cpe:/o:suse:sles:15"
```

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Platform Notes (Continued)

```
uname -a:
   Linux linux-75co 4.12.14-25.28-default #1 SMP Wed Jan 16 20:00:47 UTC 2019 (dd6077c)
   x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault):        Not affected
Microarchitectural Data Sampling:         No status reported
CVE-2017-5754 (Meltdown):                 Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled
                                          via prctl and seccomp
CVE-2017-5753 (Spectre variant 1):        Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2):        Mitigation: Enhanced IBRS, IBPB: conditional,
                                          RSB filling

run-level 3 Nov 6 07:12

SPEC is set to: /home/cpu2017
   Filesystem     Type  Size  Used Avail Use% Mounted on
   /dev/sda3      xfs   177G   94G   84G  53% /home

From /sys/devices/virtual/dmi/id
    BIOS:    Cisco Systems, Inc. C480M5.4.0.4g.0.0712190013 07/12/2019
    Vendor:  Cisco Systems Inc
    Product: UCSC-C480-M5
    Serial:  FCH2223W00A

Additional information from dmidecode follows.  WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
  Memory:
    48x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2666

(End of data from sysinfo program)
```

Compiler Version Notes

```
==============================================================================
C               | 519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------
```

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Compiler Version Notes (Continued)

```
==============================================================================
C++              | 508.namd_r(base) 510.parest_r(base)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C++, C           | 511.povray_r(base) 526.blender_r(base)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C++, C, Fortran | 507.cactuBSSN_r(base)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------

==============================================================================
Fortran          | 503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------

==============================================================================
Fortran, C       | 521.wrf_r(base) 527.cam4_r(base)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
```

(Continued on next page)

Compiler Version Notes (Continued)

```
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------
```

Base Compiler Invocation

C benchmarks:
`icc -m64 -std=c11`

C++ benchmarks:
`icpc -m64`

Fortran benchmarks:
`ifort -m64`

Benchmarks using both Fortran and C:
`ifort -m64 icc -m64 -std=c11`

Benchmarks using both C and C++:
`icpc -m64 icc -m64 -std=c11`

Benchmarks using Fortran, C, and C++:
`icpc -m64 icc -m64 -std=c11 ifort -m64`

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

C++ benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.html
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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