## SPEC CPU®2017 Floating Point Rate Result

### Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)

**DIT400TR-55R/55RL**
(2.10 GHz, Intel Xeon Silver 4216)

**SPECrates**
- SPECrate®2017_fp_base = 165
- SPECrate®2017_fp_peak = 167

<table>
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<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>SPECrate®2017_fp_base</th>
<th>SPECrate®2017_fp_peak</th>
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<tr>
<td>503.bwaves_r</td>
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<td>131</td>
<td>167</td>
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<tr>
<td>507.cactuBSSN_r</td>
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<td>131</td>
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<td>508.namd_r</td>
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<td>527.cam4_r</td>
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<td>538.imagick_r</td>
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<td>549.fotonik3d_r</td>
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</tr>
<tr>
<td>554.roms_r</td>
<td>64</td>
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<td>167</td>
</tr>
</tbody>
</table>

### Hardware
- **CPU Name:** Intel Xeon Silver 4216
- **Max MHz:** 3200
- **Nominal:** 2100
- **Enabled:** 32 cores, 2 chips, 2 threads/core
- **Orderable:** 1, 2 (chip)s
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **Cache L2:** 1 MB I+D on chip per core
- **Cache L3:** 22 MB I+D on chip per chip
- **Other:** None
- **Memory:** 384 GB (12 x 32 GB 2Rx4 PC4-2933Y-R, running at 2400)
- **Storage:** 1 x 480 GB SSD
- **Other:** None

### Software
- **OS:** CentOS Linux release 7.7.1908 (Core)
- **Compiler:** C/C++: Version 19.0.4.243 of Intel C/C++ Compiler Build 20190416 for Linux;
  Fortran: Version 19.0.4.243 of Intel Fortran Compiler Build 20190416 for Linux
- **Parallel:** No
- **Firmware:** Version V8.101 released Aug-2019
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** None
- **Power Management:** Default

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**Notes:**
- Test Date: Feb-2020
- Hardware Availability: Sep-2019
- Software Availability: Aug-2019
- Test Sponsor: Netweb Pte Ltd
- **Tyrone Systems**
- **DIT400TR-55R/55RL** (2.10 GHz, Intel Xeon Silver 4216)

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Copyright 2017-2020 Standard Performance Evaluation Corporation
Results Table

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<tr>
<th>Benchmark</th>
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<th>Ratio</th>
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</tr>
</tbody>
</table>

**Compiler Notes**

SPEC has learned that this result, which used an evaluation compiler, was submitted contrary to the compiler license terms.

Intel has granted a one-time waiver for this result.

**Submit Notes**

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.

For details, please see the config file.

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

**Environment Variables Notes**

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"
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(Test Sponsor: Netweb Pte Ltd)  
DIT400TR-55R/55RL  
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<tr>
<td>Tested by: Netweb</td>
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</table>

SPECrate®2017_fp_base = 165
SPECrate®2017_fp_peak = 167

CPU2017 License: 006042  
Test Date: Feb-2020

Test Sponsor: Netweb Pte Ltd  
Hardware Availability: Sep-2019

Tested by: Netweb  
Software Availability: Aug-2019

**General Notes**

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

test_date

runcpu command invoked through numactl i.e.:

numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

**Platform Notes**

Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r6365 of 2019-08-21 295195f888a3d7eb16e46a485a0011
running on NODE6 Wed Oct 9 03:13:48 2019

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see

https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Silver 4216 CPU @ 2.10GHz
2  "physical id"s (chips)
64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
siblings : 32
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
```

From lscpu:

```
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 64
On-line CPU(s) list: 0-63
Thread(s) per core: 2
Core(s) per socket: 16
Socket(s): 2
```

(Continued on next page)
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CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Netweb

Specrate 2017_fp_peak = 167
Specrate 2017_fp_base = 165

Platform Notes (Continued)

NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4216 CPU @ 2.10GHz
Stepping: 7
CPU MHz: 799.932
CPU max MHz: 3200.0000
CPU min MHz: 800.0000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 22528K
NUMA node0 CPU(s): 0-15,32-47
NUMA node1 CPU(s): 16-31,48-63

Flags:
  fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
  pat pse36 clflush dts acpica mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
  lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
  aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
  fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
  xsave avx f16c rdrand lahf_lm abm 3nowprefetch ebpx cat_13 cdp_l3 intel_pinn
  intel_pt ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vmmi flexpriority ept
  vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdtp
  avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt
  xsaves xgetbv1 cqm_l1c cqm_occupp_l1c cqm_mmb_total cqm_mmb_local dtherm ida arat
  pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pu ospke avx512_vnni md_clear spec_ctrl
  intel_stibp flush_l1d arch_capabilities

/proc/cpuinfo cache data
  cache size : 22528 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 2 nodes (0-1)
    node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 32 33 34 35 36 37 38 39 40 41 42 43
    node 0 size: 195228 MB
    node 0 free: 174368 MB
    node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 48 49 50 51 52 53 54 55 56
    node 1 size: 196608 MB
    node 1 free: 177807 MB
    node distances:
      node 0 1
      0: 10 21

(Continued on next page)
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SPECRate®2017_fp_base = 165
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CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Netweb

Platform Notes (Continued)

1: 21 10

From /proc/meminfo
MemTotal: 394671656 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release*/etc/*version*
centos-release: CentOS Linux release 7.7.1908 (Core)
centos-release-upstream: Derived from Red Hat Enterprise Linux 7.7 (Source)

os-release:
NAME="CentOS Linux"
VERSION="7 (Core)"
ID="centos"
ID_LIKE="rhel fedora"
VERSION_ID="7"
PRETTY_NAME="CentOS Linux 7 (Core)"
ANSI_COLOR="0;31"
CPE_NAME="cpe:/o:centos:centos:7"
redhat-release: CentOS Linux release 7.7.1908 (Core)
system-release: CentOS Linux release 7.7.1908 (Core)
system-release-cpe: cpe:/o:centos:centos:7

uname -a:
Linux NODE6 3.10.0-1062.el7.x86_64 #1 SMP Wed Aug 7 18:08:02 UTC 2019 x86_64 x86_64
x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: Load fences, __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Full retpoline, IBPB

run-level 3 Oct 8 17:25
SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/mapper/centos-home xfs 392G 196G 197G 50% /home

From /sys/devices/virtual/dmi/id
BIOS: American Megatrends Inc. V8.101 08/02/2019
Vendor: Tyrone Systems

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CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Netweb

Platform Notes (Continued)

Product: DIT400TR-55R
Serial: empty

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

(End of data from sysinfo program)

Compiler Version Notes

=======================================================================================================
C               | 519.lbm_r(base, peak) 538.imagick_r(base, peak)
| 544.nab_r(base, peak)
=======================================================================================================
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.243 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
icc: NOTE: The evaluation period for this product ends on 2-nov-2019 UTC.

=======================================================================================================
C++             | 508.namd_r(base, peak) 510.parest_r(base, peak)
=======================================================================================================
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.243 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
icpc: NOTE: The evaluation period for this product ends on 2-nov-2019 UTC.

=======================================================================================================
C++, C          | 511.povray_r(base, peak) 526.blender_r(base, peak)
=======================================================================================================
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.243 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
icpc: NOTE: The evaluation period for this product ends on 2-nov-2019 UTC.

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.243 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
icc: NOTE: The evaluation period for this product ends on 2-nov-2019 UTC.

=======================================================================================================
C++, C, Fortran | 507.cactuBSSN_r(base, peak)
(Continued on next page)
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CPU2017 License: 006042
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Tested by: Netweb

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Compiler Version Notes (Continued)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.243 Build 20190416
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icpc: NOTE: The evaluation period for this product ends on 2-nov-2019 UTC.
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icc: NOTE: The evaluation period for this product ends on 2-nov-2019 UTC.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.243 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
ifort: NOTE: The evaluation period for this product ends on 2-nov-2019 UTC.

==============================================================================
Fortran         | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
| 554.roms_r(base, peak)
==============================================================================

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.243 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
ifort: NOTE: The evaluation period for this product ends on 2-nov-2019 UTC.

==============================================================================
Fortran, C      | 521.wrf_r(base, peak) 527.cam4_r(base, peak)
==============================================================================

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.243 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
ifort: NOTE: The evaluation period for this product ends on 2-nov-2019 UTC.

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Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

(Continued on next page)
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SPECrater®2017.fp_base = 165
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CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Netweb

Base Compiler Invocation (Continued)

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbmr_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

C++ benchmarks:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

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Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
DIT400TR-55R/55RL
(2.10 GHz, Intel Xeon Silver 4216)

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Netweb

SPECrate®2017_fp_base = 165
SPECrate®2017_fp_peak = 167

Test Date: Feb-2020
Hardware Availability: Sep-2019
Software Availability: Aug-2019

Base Optimization Flags (Continued)

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags

Same as Base Portability Flags
## Peak Optimization Flags

### C benchmarks:

519.lbm_r: `-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4`

538.imagick_r: `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4`

544.nab_r: Same as 538.imagick_r

### C++ benchmarks:

508.namd_r: `-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4`

510.parest_r: `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4`

### Fortran benchmarks:

503.bwaves_r: `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs -align array32byte`

549.fotonik3d_r: Same as 503.bwaves_r

554.roms_r: `-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs -align array32byte`

### Benchmarks using both Fortran and C:

- `prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs -align array32byte`

### Benchmarks using both C and C++:

511.povray_r: `-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4`

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SPEC CPU®2017 Floating Point Rate Result

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Peak Optimization Flags (Continued)

526.blender_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/TyroneIT-Platform-Settings-V1-CLX-revA.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/TyroneIT-Platform-Settings-V1-CLX-revA.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.0 on 2019-10-08 17:43:47-0400.
Originally published on 2020-03-17.