Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6240R, 2.40GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base = 249</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_peak = 253</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

CPU Name: Intel Xeon Gold 6240R
Max MHz: 4000
Nominal: 2400
Enabled: 48 cores, 2 chips, 2 threads/core
Orderable: 1,2 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 35.75 MB I+D on chip per chip
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
Storage: 1 x 960 GB SSD SAS
Other: None

OS: SUSE Linux Enterprise Server 15 (x86_64)
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux

Parallel: No
Firmware: Version 4.0.4j released Aug-2019
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Power Management: BIOS set to prefer performance at the cost of additional power usage

Test Date: Feb-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

<table>
<thead>
<tr>
<th>Copies</th>
<th>SPECrate®2017_fp_base (249)</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r 96</td>
<td>209</td>
</tr>
<tr>
<td>507.cactuBSSN_r 96</td>
<td>209</td>
</tr>
<tr>
<td>508.namd_r 96</td>
<td>212</td>
</tr>
<tr>
<td>510.parest_r 96</td>
<td>130</td>
</tr>
<tr>
<td>511.povray_r 96</td>
<td>309</td>
</tr>
<tr>
<td>519.lbm_r 96</td>
<td>128</td>
</tr>
<tr>
<td>521.wrf_r 96</td>
<td>231</td>
</tr>
<tr>
<td>526.blender_r 96</td>
<td>294</td>
</tr>
<tr>
<td>527.cam4_r 96</td>
<td>230</td>
</tr>
<tr>
<td>538.imagick_r 96</td>
<td>359</td>
</tr>
<tr>
<td>544.nab_r 96</td>
<td>428</td>
</tr>
<tr>
<td>549.fotonik3d_r 96</td>
<td>169</td>
</tr>
<tr>
<td>554.roms_r 96</td>
<td>104</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_peak (253)</th>
</tr>
</thead>
<tbody>
<tr>
<td>536</td>
</tr>
<tr>
<td>535</td>
</tr>
<tr>
<td>666</td>
</tr>
<tr>
<td>472</td>
</tr>
<tr>
<td>478</td>
</tr>
<tr>
<td>169</td>
</tr>
<tr>
<td>169</td>
</tr>
<tr>
<td>104</td>
</tr>
<tr>
<td>104</td>
</tr>
</tbody>
</table>
## SPEC CPU®2017 Floating Point Rate Result

**Cisco Systems**

Cisco UCS C240 M5 (Intel Xeon Gold 6240R, 2.40GHz)

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**SPECrate®2017_fp_base = 249**  
**SPECrate®2017_fp_peak = 253**

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>96</td>
<td>1799</td>
<td>535</td>
<td>1798</td>
<td>535</td>
<td>1797</td>
<td>536</td>
<td>96</td>
<td>1798</td>
<td>536</td>
<td>1797</td>
<td>536</td>
<td>1797</td>
<td>536</td>
<td></td>
<td></td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>96</td>
<td>580</td>
<td>209</td>
<td>580</td>
<td>209</td>
<td>581</td>
<td>209</td>
<td>96</td>
<td>580</td>
<td>209</td>
<td>581</td>
<td>209</td>
<td>582</td>
<td>209</td>
<td></td>
<td></td>
</tr>
<tr>
<td>508.namd_r</td>
<td>96</td>
<td>435</td>
<td>121</td>
<td>431</td>
<td>122</td>
<td>431</td>
<td>122</td>
<td>96</td>
<td>428</td>
<td>123</td>
<td>427</td>
<td>124</td>
<td>428</td>
<td>124</td>
<td></td>
<td></td>
</tr>
<tr>
<td>510.parest_r</td>
<td>96</td>
<td>1928</td>
<td>130</td>
<td>1932</td>
<td>130</td>
<td>1926</td>
<td>130</td>
<td>96</td>
<td>1934</td>
<td>131</td>
<td>1924</td>
<td>131</td>
<td>1929</td>
<td>130</td>
<td></td>
<td></td>
</tr>
<tr>
<td>511.povray_r</td>
<td>96</td>
<td>727</td>
<td>308</td>
<td>726</td>
<td>309</td>
<td>726</td>
<td>309</td>
<td>96</td>
<td>623</td>
<td>360</td>
<td>625</td>
<td>359</td>
<td>625</td>
<td>359</td>
<td></td>
<td></td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>96</td>
<td>790</td>
<td>128</td>
<td>790</td>
<td>128</td>
<td>790</td>
<td>128</td>
<td>96</td>
<td>790</td>
<td>128</td>
<td>790</td>
<td>128</td>
<td>790</td>
<td>128</td>
<td></td>
<td></td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>96</td>
<td>922</td>
<td>233</td>
<td>931</td>
<td>231</td>
<td>932</td>
<td>231</td>
<td>96</td>
<td>918</td>
<td>234</td>
<td>909</td>
<td>237</td>
<td>906</td>
<td>237</td>
<td></td>
<td></td>
</tr>
<tr>
<td>526.blender_r</td>
<td>96</td>
<td>498</td>
<td>294</td>
<td>499</td>
<td>293</td>
<td>498</td>
<td>294</td>
<td>96</td>
<td>497</td>
<td>294</td>
<td>498</td>
<td>294</td>
<td>498</td>
<td>293</td>
<td></td>
<td></td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>96</td>
<td>549</td>
<td>306</td>
<td>549</td>
<td>306</td>
<td>547</td>
<td>307</td>
<td>96</td>
<td>540</td>
<td>311</td>
<td>540</td>
<td>311</td>
<td>537</td>
<td>313</td>
<td></td>
<td></td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>96</td>
<td>357</td>
<td>668</td>
<td>359</td>
<td>665</td>
<td>357</td>
<td>668</td>
<td>96</td>
<td>358</td>
<td>666</td>
<td>359</td>
<td>665</td>
<td>358</td>
<td>667</td>
<td></td>
<td></td>
</tr>
<tr>
<td>544.nab_r</td>
<td>96</td>
<td>344</td>
<td>470</td>
<td>338</td>
<td>478</td>
<td>338</td>
<td>479</td>
<td>96</td>
<td>338</td>
<td>477</td>
<td>342</td>
<td>472</td>
<td>342</td>
<td>472</td>
<td></td>
<td></td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>96</td>
<td>2209</td>
<td>169</td>
<td>2206</td>
<td>170</td>
<td>2208</td>
<td>169</td>
<td>96</td>
<td>2208</td>
<td>169</td>
<td>2208</td>
<td>169</td>
<td>2206</td>
<td>170</td>
<td></td>
<td></td>
</tr>
<tr>
<td>554.roms_r</td>
<td>96</td>
<td>1461</td>
<td>104</td>
<td>1462</td>
<td>104</td>
<td>1462</td>
<td>104</td>
<td>96</td>
<td>1460</td>
<td>104</td>
<td>1466</td>
<td>104</td>
<td>1463</td>
<td>104</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Results Table**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## Environment Variables Notes

Environment variables set by runcpu before the start of the run:  
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"

## General Notes

Binaries compiled on a system with 1x Intel Core i9–7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Filesystem page cache synced and cleared with:  
sync; echo 3> /proc/sys/vm/drop_caches

(Continued on next page)
Cisco Systems  
Cisco UCS C240 M5 (Intel Xeon Gold 6240R, 2.40GHz)  

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base = 249</th>
<th>SPECrate®2017_fp_peak = 253</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU2017 License: 9019</td>
<td>Test Date: Feb-2020</td>
</tr>
<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>Hardware Availability: Feb-2020</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: May-2019</td>
</tr>
</tbody>
</table>

General Notes (Continued)

runcpu command invoked through numactl i.e.:  
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r6365 of 2019-08-21 295195f888a3d7ed1e6e46a485a0011  
runtime linux-4z0x Wed Feb 5 11:31:08 2020

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see  
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo  
model name : Intel(R) Xeon(R) Gold 6240R CPU @ 2.40GHz  
2 "physical id"s (chips)  
96 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 24  
siblings : 48  
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29  
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29

From lscpu:  
Architecture: x86_64  
CPU op-mode(s): 32-bit, 64-bit  
Byte Order: Little Endian  
CPU(s): 96  
On-line CPU(s) list: 0-95  
Thread(s) per core: 2  
Core(s) per socket: 24  
Socket(s): 2  
NUMA node(s): 4
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6240R, 2.40GHz)

SPECrater®2017_fp_base = 249
SPECrater®2017_fp_peak = 253

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Feb-2020
Tested by: Cisco Systems
Hardware Availability: Feb-2020
Software Availability: May-2019

Platform Notes (Continued)

Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6240R CPU @ 2.40GHz
Stepping: 7
CPU MHz: 2400.000
CPU max MHz: 4000.0000
CPU min MHz: 1000.0000
BogoMIPS: 4800.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 36608K
NUMA node0 CPU(s): 0-3,7-9,13-15,19,20,24-30,34-36,40-42,45-47,76-78,82-84,88-90,93-95
NUMA node1 CPU(s): 4-6,10-12,16-18,21-23,52-54,58-60,64-66,69-71
NUMA node2 CPU(s): 24-27,31-33,37-39,43,44,72-75,79-81,85-87,91,92
NUMA node3 CPU(s): 28-30,34-36,40-42,45-47,76-78,82-84,88-90,93-95
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtsscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmerge tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 x86ti pdcm pclid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_13 cdp_l3 invpcid_single intel_pinn mba tpr_shadow vmx flexpriority ept
vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ibrms invpcid rtm cqm mpx rdt_a
avx512if avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsave xgetbv1 xsavec cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local
ibpb ibr nstibp dtcmon ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospke avx512_vnni arch_capabilities ssbd

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 7 8 9 13 14 15 19 20 48 49 50 51 55 56 57 61 62 63 67 68
node 0 size: 192102 MB
node 0 free: 178677 MB
node 1 cpus: 4 5 6 10 11 12 16 17 18 21 22 23 52 53 54 58 59 60 64 65 66 69 70 71
node 1 size: 193526 MB
node 1 free: 183356 MB
node 2 cpus: 24 25 26 27 31 32 33 37 38 39 43 44 72 73 74 75 79 80 81 85 86 87 91 92
node 2 size: 193526 MB
node 2 free: 183578 MB
node 3 cpus: 28 29 30 34 35 36 40 41 42 45 46 47 76 77 78 82 83 84 88 89 90 93 94 95

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6240R, 2.40GHz)

SPEC CPU®2017 Floating Point Rate Result

**SPECrate®2017_fp_base = 249**

**SPECrate®2017_fp_peak = 253**

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Feb-2020  
**Hardware Availability:** Feb-2020  
**Software Availability:** May-2019

---

**Platform Notes (Continued)**

node 3 size: 193494 MB  
node 3 free: 183553 MB  
node distances:

<table>
<thead>
<tr>
<th></th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>10</td>
<td>11</td>
<td>21</td>
<td>21</td>
</tr>
<tr>
<td>1</td>
<td>11</td>
<td>10</td>
<td>21</td>
<td>21</td>
</tr>
<tr>
<td>2</td>
<td>21</td>
<td>21</td>
<td>10</td>
<td>11</td>
</tr>
<tr>
<td>3</td>
<td>21</td>
<td>21</td>
<td>11</td>
<td>10</td>
</tr>
</tbody>
</table>

From /proc/meminfo

- MemTotal: 791192812 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*

- os-release:
  - NAME="SLES"
  - VERSION="15"
  - VERSION_ID="15"
  - PRETTY_NAME="SUSE Linux Enterprise Server 15"
  - ID="sles"
  - ID_LIKE="suse"
  - ANSI_COLOR="0;32"
  - CPE_NAME="cpe:/o:suse:sles:15"

uname -a:

Linux linux-4z0x 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)  
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

- CVE-2018-3620 (L1 Terminal Fault): No status reported
- Microarchitectural Data Sampling: No status reported
- CVE-2017-5754 (Meltdown): Not affected
- CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
- CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
- CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Feb 5 02:47

SPEC is set to: /home/cpu2017

<table>
<thead>
<tr>
<th>Filesystem</th>
<th>Type</th>
<th>Size</th>
<th>Used</th>
<th>Avail</th>
<th>Use%</th>
<th>Mounted on</th>
</tr>
</thead>
<tbody>
<tr>
<td>/dev/sdaf1</td>
<td>xfs</td>
<td>891G</td>
<td>90G</td>
<td>801G</td>
<td>11%</td>
<td>/</td>
</tr>
</tbody>
</table>

From /sys/devices/virtual/dmi/id

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6240R, 2.40GHz)

SPECrate®2017_fp_base = 249
SPECrate®2017_fp_peak = 253

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Feb-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

Platform Notes (Continued)

BIOS: Cisco Systems, Inc. C240M5.4.0.4j.0.0831191216 08/31/2019
Vendor: Cisco Systems Inc
Product: UCSC-C240-M5L
Serial: WZP21460GO8

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
| C | 519.lbm_r(base, peak) 538.imagick_r(base, peak) 544.nab_r(base, peak) |
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================

==============================================================================
| C++ | 508.namd_r(base, peak) 510.parest_r(base, peak) |
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================

==============================================================================
| C++, C | 511.povray_r(base, peak) 526.blender_r(base, peak) |
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================

==============================================================================
| C++, C, Fortran | 507.cactuBSSN_r(base, peak) |
(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6240R, 2.40GHz)

**SPECrate®2017_fp_base = 249**
**SPECrate®2017_fp_peak = 253**

| Test Date: | Feb-2020 |
| Test Sponsor: | Cisco Systems |
| Tested by: | Cisco Systems |
| Hardware Availability: | Feb-2020 |
| Software Availability: | May-2019 |

---

### Compiler Version Notes (Continued)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---

<table>
<thead>
<tr>
<th>Fortran</th>
<th>503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak) 554.roms_r(base, peak)</th>
</tr>
</thead>
</table>

---

<table>
<thead>
<tr>
<th>Fortran, C</th>
<th>521.wrf_r(base, peak) 527.cam4_r(base, peak)</th>
</tr>
</thead>
</table>

---

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---

### Base Compiler Invocation

C benchmarks:
```bash
icc -m64 -std=c11
```

C++ benchmarks:
```bash
icpc -m64
```

Fortran benchmarks:
```bash
ifort -m64
```

Benchmarks using both Fortran and C:
```bash
ifort -m64 icc -m64 -std=c11
```

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6240R, 2.40GHz)

SPECrate®2017_fp_base = 249
SPECrate®2017_fp_peak = 253

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Feb-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

Base Compiler Invocation (Continued)

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

C++ benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6240R, 2.40GHz)

SPECrate®2017_fp_base = 249
SPECrate®2017_fp_peak = 253

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Feb-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

Base Optimization Flags (Continued)

Benchmarks using both C and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
519.blm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
- qopt-mem-layout-trans=4

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6240R, 2.40GHz)  

peak Optimization Flags (Continued)

538.imagick_r: -xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4

544.nab_r: Same as 538.imagick_r

C++ benchmarks:

508.namd_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -03 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4

510.parest_r: -xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:

503.bwaves_r: -xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs -align array32byte

549.fotonik3d_r: Same as 503.bwaves_r

554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -03 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:

- prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -03 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -03 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4

526.blender_r: -xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:

-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6240R, 2.40GHz)

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>SPECrate®2017_fp_base =</td>
<td>249</td>
</tr>
<tr>
<td>SPECrate®2017_fp_peak =</td>
<td>253</td>
</tr>
<tr>
<td>Test Date:</td>
<td>Feb-2020</td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Feb-2020</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>May-2019</td>
</tr>
</tbody>
</table>

**Peak Optimization Flags (Continued)**

Benchmarks using Fortran, C, and C++ (continued):

-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.0 on 2020-02-05 01:01:07-0500.
Originally published on 2020-03-17.