**SPEC CPU®2017 Integer Rate Result**

**Hewlett Packard Enterprise**
(Test Sponsor: HPE)
Synergy 480 Gen10
(3.10 GHz, Intel Xeon Gold 6242R)

**SPECrates®2017_int_base = 272**  
**SPECrates®2017_int_peak = 283**

| Software         | OS: SUSE Linux Enterprise Server 15 SP1 (x86_64)  
|                 | Kernel 4.12.14-195-defautl  
|                 | Compiler: C/C++: Version 19.0.4.227 of Intel C/C++  
|                 | Compiler Build 20190416 for Linux;  
|                 | Fortran: Version 19.0.4.227 of Intel Fortran  
|                 | Compiler Build 20190416 for Linux;  
|                 | Parallel: No  
|                 | Firmware: HPE BIOS Version I42 v2.22 (11/13/2019) released Feb-2020  
|                 | File System: btrfs  
|                 | System State: Run level 3 (multi-user)  
|                 | Base Pointers: 64-bit  
|                 | Peak Pointers: 32/64-bit  
|                 | Other: jemalloc memory allocator V5.0.1  
|                 | Power Management: BIOS set to prefer performance at the cost of additional power usage  

| Hardware         | CPU Name: Intel Xeon Gold 6242R  
|                 | Max MHz: 4100  
|                 | Nominal: 3100  
|                 | Enabled: 40 cores, 2 chips, 2 threads/core  
|                 | Orderable: 1, 2 chip(s)  
|                 | Cache L1: 32 KB I + 32 KB D on chip per core  
|                 | L2: 1 MB I+D on chip per core  
|                 | L3: 35.75 MB I+D on chip per chip  
|                 | Other: None  
|                 | Memory: 384 GB (24 x 16 GB 2Rx8 PC4-2933Y-R)  
|                 | Storage: 1 x 400 GB SAS SSD, RAID 0  
|                 | Other: None  

<table>
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<tr>
<th>Copied</th>
<th>SPECrate®2017_int_base (272)</th>
<th>SPECrate®2017_int_peak (283)</th>
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Results Table

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</tr>
</tbody>
</table>

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Files system page cache synced and cleared with:  
sync; echo 3 > /proc/sys/vm/drop_caches

Environment Variables Notes

Environment variables set by runcpu before the start of the run:  
LD_LIBRARY_PATH =  
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM  
memory using Redhat Enterprise Linux 7.5  
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
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CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

General Notes (Continued)

is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Configuration:
Thermal Configuration set to Maximum Cooling
Memory Patrol Scrubbing set to Disabled
LLC Prefetch set to Enabled
LLC Dead Line Allocation set to Disabled
Enhanced Processor Performance set to Enabled
Workload Profile set to General Throughput Compute
Workload Profile set to Custom
Energy/Performance Bias set to Balanced Performance

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7ed1e6e46a485a0011
running on linux-96aw Sat Feb 29 02:53:08 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Gold 6242R CPU @ 3.10GHz
  2 "physical id"s (chips)
  80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 20
siblings : 40
physical 0: cores 1 2 3 5 8 9 10 12 13 16 17 18 19 20 21 26 27 28 29
physical 1: cores 0 1 2 3 5 8 9 10 12 13 16 18 19 20 21 26 27 28 29

From lscpu:
Architecture:        x86_64
CPU op-mode(s):      32-bit, 64-bit
Byte Order:          Little Endian
Address sizes:       46 bits physical, 48 bits virtual
CPU(s):              80

(Continued on next page)
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**Test Sponsor:** HPE  
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**Platform Notes (Continued)**

On-line CPU(s) list: 0–79  
Thread(s) per core: 2  
Core(s) per socket: 20  
Socket(s): 2  
NUMA node(s): 4  
Vendor ID: GenuineIntel  
CPU family: 6  
Model: 85  
Model name: Intel(R) Xeon(R) Gold 6242R CPU @ 3.10GHz  
Stepping: 7  
CPU MHz: 3100.000  
BogoMIPS: 6200.00  
Virtualization: VT-x  
L1d cache: 32K  
L1i cache: 32K  
L2 cache: 1024K  
L3 cache: 36608K  
NUMA node0 CPU(s): 0–9,40–49  
NUMA node1 CPU(s): 10–19,50–59  
NUMA node2 CPU(s): 20–29,60–69  
NUMA node3 CPU(s): 30–39,70–79  

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_pwpin ssbd mba ibrs ibpb ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512v1 xsaveopt xsavec xgetbv1 xsave xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local dtherm ida arat pln pts pku ospke avx512_vnni md_clear flush_l1d arch_capabilities

/proc/cpuinfo cache data  
  cache size : 36608 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.  
  available: 4 nodes (0-3)  
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 40 41 42 43 44 45 46 47 48 49  
  node 0 size: 96286 MB  
  node 0 free: 95997 MB  
  node 1 cpus: 10 11 12 13 14 15 16 17 18 19 50 51 52 53 54 55 56 57 58 59  
  node 1 size: 96764 MB  
  node 1 free: 96337 MB  
  node 2 cpus: 20 21 22 23 24 25 26 27 28 29 60 61 62 63 64 65 66 67 68 69

(Continued on next page)
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Platform Notes (Continued)

node 2 size: 96734 MB
node 2 free: 96535 MB
node 3 cpus: 30 31 32 33 34 35 36 37 38 39 70 71 72 73 74 75 76 77 78 79
node 3 size: 96565 MB
node 3 free: 96375 MB
node distances:
node 0 1 2 3
  0:  10  21  31  31
  1:  21  10  31  31
  2:  31  31  10  21
  3:  31  31  21  10

From /proc/meminfo
MemTotal:     395623376 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
NAME="SLES"
VERSION="15-SP1"
VERSION_ID="15.1"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP1"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp1"

uname -a:
Linux linux-96aw 4.12.14-195-default #1 SMP Tue May 7 10:55:11 UTC 2019 (8fba516)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

run-level 3 Feb 29 02:51

SPEC is set to: /home/cpu2017

(Continued on next page)
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SPECrates®

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Tested by: HPE

Test Date: Feb-2020
Hardware Availability: Feb-2020
Software Availability: Jun-2019

Platform Notes (Continued)
/dev/sda2 btrfs 371G 109G 262G 30% /home

From /sys/devices/virtual/dmi/id
BIOS: HPE I42 11/13/2019
Vendor: HPE
Product: Synergy 480 Gen10
Product Family: Synergy
Serial: MXQ72204FC

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory: 24x UNKNOWN NOT AVAILABLE 16 GB 2 rank 2933

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C | 502.gcc_r(peak)

Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
C | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
   | 525.x264_r(base, peak) 557.xz_r(base, peak)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
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Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
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**CPU2017 License:** 3  
**Test Sponsor:** HPE  
**Tested by:** HPE

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**Compiler Version Notes (Continued)**

```plaintext
C      | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)  
      | 525.x264_r(base, peak) 557.xz_r(base, peak)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
C++     | 523.xalancbmk_r(peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version  
19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
C++     | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base) 531.deepsjeng_r(base, peak)  
      | 541.leela_r(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
C++     | 523.xalancbmk_r(peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version  
19.0.4.227 Build 20190416  
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==============================================================================
C++     | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base) 531.deepsjeng_r(base, peak)  
      | 541.leela_r(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
Fortran | 548.exchange2_r(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.0.4.227 Build 20190416
```

(Continued on next page)
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\begin{align*}
\text{SPECrate} \text{®2017}_\text{int}_\text{peak} &= 283 \\
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\text{Test Date: } & Feb-2020 \\
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\text{Software Availability: } & Jun-2019 \\
\end{tabular}

 Compiler Version Notes (Continued)

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\section*{Base Compiler Invocation}

C benchmarks:
\begin{verbatim}
icc -m64 -std=c11
\end{verbatim}

C++ benchmarks:
\begin{verbatim}
icpc -m64
\end{verbatim}

Fortran benchmarks:
\begin{verbatim}
ifort -m64
\end{verbatim}

\section*{Base Portability Flags}

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

\section*{Base Optimization Flags}

C benchmarks:
\begin{verbatim}
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
\end{verbatim}

C++ benchmarks:
\begin{verbatim}
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
\end{verbatim}

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Test Date: Feb-2020
Hardware Availability: Feb-2020
Software Availability: Jun-2019

Base Optimization Flags (Continued)

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m64 -std=c11


C++ benchmarks (except as noted below):
icpc -m64

523.xalancbmk_r:icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin

Fortran benchmarks:
ifort -m64

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:
500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4

(Continued on next page)
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Test Sponsor: HPE
Tested by: HPE

Peak Optimization Flags (Continued)

500.perlbench_r (continued):
   -fno-strict-overflow
   -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
   -lqkmalloc

502.gcc_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
   -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
   -L/usr/local/jie5.0.1-32/lib -ljemalloc

505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
   -qopt-mem-layout-trans=4
   -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
   -lqkmalloc

525.x264_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
   -qopt-mem-layout-trans=4 -fno-alias
   -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
   -lqkmalloc

557.xz_r: Same as 505.mcf_r

C++ benchmarks:

520.omnetpp_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
   -qopt-mem-layout-trans=4
   -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
   -lqkmalloc

523.xalancbmk_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
   -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
   -L/usr/local/jie5.0.1-32/lib -ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
   -qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
   -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
   -lqkmalloc

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.html
Hewlett Packard Enterprise
(Test Sponsor: HPE)
Synergy 480 Gen10
(3.10 GHz, Intel Xeon Gold 6242R)

SPECrate®2017_int_base = 272
SPECrate®2017_int_peak = 283

CPU2017 License: 3
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You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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