## Hardware

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
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<tr>
<td>perlbench_r</td>
<td>40</td>
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<td>gcc_r</td>
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<td>omnetpp_r</td>
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<td>xalancbmk_r</td>
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<td>x264_r</td>
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<td>deepsjeng_r</td>
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<tr>
<td>xz_r</td>
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## Software

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<thead>
<tr>
<th>OS</th>
<th>SUSE Linux Enterprise Server 15 SP1 (x86_64)</th>
<th>Kernel 4.12.14-195-default</th>
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<td>Compiler</td>
<td>C/C++: Version 19.0.4.227 of Intel C/C++ Compiler Build 20190416 for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler Build 20190416 for Linux;</td>
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<tr>
<td>Firmware</td>
<td>HPE BIOS Version U32 v2.22 (11/13/2019) released Apr-2020</td>
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<td>System State</td>
<td>Run level 3 (multi-user)</td>
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<tr>
<td>Base Pointers</td>
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<tr>
<td>Power Management</td>
<td>BIOS set to prefer performance at the cost of additional power usage</td>
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Copyright 2017-2020 Standard Performance Evaluation Corporation
## SPEC CPU®2017 Integer Rate Result

### Results Table

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<th>Seconds</th>
<th>Ratio</th>
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<td>583</td>
<td>74.1</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

- Stack size set to unlimited using "ulimit -s unlimited"
- Transparent Huge Pages enabled by default
- Prior to runcpu invocation
- Filesystem page cache synced and cleared with:
  ```
  sync; echo 3 > /proc/sys/vm/drop_caches
  ```

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:
```
LD_LIBRARY_PATH = "/cpu2017/lib/intel64:/cpu2017/lib/ia32:/cpu2017/je5.0.1-32"
```

### General Notes

- Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
- NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
- Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
**SPEC CPU®2017 Integer Rate Result**

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**Hewlett Packard Enterprise**
(Test Sponsor: HPE)
ProLiant DL360 Gen10
(2.40 GHz, Intel Xeon Silver 4210R)

**SPECrate®2017_int_base** = 114
**SPECrate®2017_int_peak** = 119

---

**General Notes (Continued)**

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.


---

**Platform Notes**

BIOS Configuration:
- Thermal Configuration set to Maximum Cooling
- Memory Patrol Scrubbing set to Disabled
- LLC Prefetch set to Enabled
- LLC Dead Line Allocation set to Disabled
- Enhanced Processor Performance set to Enabled
- Workload Profile set to General Throughput Compute
- Workload Profile set to Custom
- Energy/Performance Bias set to Balanced Performance

Sysinfo program /cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7ed8b1e6e46a485a0011
running on linux-9e60 Wed Mar 4 12:51:10 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Silver 4210R CPU @ 2.40GHz
2 "physical id"s (chips)
40 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 10
siblings : 20
physical 0: cores 0 1 2 3 4 8 9 10 11 12
physical 1: cores 0 1 2 3 4 8 9 10 11 12
```

From lscpu:

```
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 48 bits virtual
CPU(s): 40
On-line CPU(s) list: 0-39
Thread(s) per core: 2
Core(s) per socket: 10
```

(Continued on next page)
Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL360 Gen10
(2.40 GHz, Intel Xeon Silver 4210R)

SPECrate®2017_int_base = 114
SPECrate®2017_int_peak = 119

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Platform Notes (Continued)

Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4210R CPU @ 2.40GHz
Stepping: 7
CPU MHz: 2400.000
BogoMIPS: 4800.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 14080K
NUMA node0 CPU(s): 0-9,20-29
NUMA node1 CPU(s): 10-19,30-39

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3
invpnc_single intel_p钎n ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi
flexpriority ept vpid fsgsbase tsc_adjust bm1 hle avx2 smep bmi2 erms invpcid rtm
cqmx mpx rdt_a avxv512f avxv512dq rdseed adx clflushopt clwb intel_pt avxv512cd
avxv512bw avxv512vl xsaveopt xsavec xgetbv1 xsaves cqmx_l1c cqmx_occup_l1c cqmx_mb_total
cqmx_mb_local dtherm ida arat pln pts pku ospke avxv512_vnni md_clear flush_lld
arch_capabilities

From /proc/cpuinfo cache data

/cache size : 14080 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.

available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 20 21 22 23 24 25 26 27 28 29
node 0 size: 193097 MB
node 0 free: 190766 MB
node 1 cpus: 10 11 12 13 14 15 16 17 18 19 30 31 32 33 34 35 36 37 38 39
node 1 size: 193531 MB
node 1 free: 193122 MB
node distances:
node 0 1
0: 10 21
1: 21 10

From /proc/meminfo

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL360 Gen10
(2.40 GHz, Intel Xeon Silver 4210R)

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

SPECrate®2017_int_base = 114
SPECrate®2017_int_peak = 119

Test Date: Mar-2020
Hardware Availability: Apr-2020
Software Availability: Jun-2019

Platform Notes (Continued)

MemTotal: 395907720 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
    os-release:
      NAME="SLES"
      VERSION="15-SP1"
      VERSION_ID="15.1"
      PRETTY_NAME="SUSE Linux Enterprise Server 15 SP1"
      ID="sles"
      ID_LIKE="suse"
      ANSI_COLOR="0;32"
      CPE_NAME="cpe:/o:suse:sles:15:sp1"

uname -a:
    Linux linux-9e6o 4.12.14-195-default #1 SMP Tue May 7 10:55:11 UTC 2019 (8fba516)
    x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

run-level 3 Mar 4 12:48

SPEC is set to: /cpu2017
    Filesystem  Type  Size  Used Avail Use% Mounted on
    /dev/sda2  btrfs  369G  137G  233G  37% /

From /sys/devices/virtual/dmi/id
    BIOS: HPE U32 11/13/2019
    Vendor: HPE
    Product: ProLiant DL360 Gen10
    Product Family: ProLiant
    Serial: MXQ94204PS

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL360 Gen10
(2.40 GHz, Intel Xeon Silver 4210R)

SPECrate®2017_int_base = 114
SPECrate®2017_int_peak = 119

Platform Notes (Continued)

Memory:
24x UNKNOWN NOT AVAILABLE 16 GB 2 rank 2933

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C       | 502.gcc_r(peak)
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
C       | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
        | 525.x264_r(base, peak) 557.xz_r(base, peak)
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
C       | 502.gcc_r(peak)
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
C++     | 523.xalancbmk_r(peak)
Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416

(Continued on next page)
Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL360 Gen10
(2.40 GHz, Intel Xeon Silver 4210R)

SPEC CPU®2017 Integer Rate Result
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SPECrate®2017_int_base = 114
SPECrate®2017_int_peak = 119

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Test Date: Mar-2020
Hardware Availability: Apr-2020
Software Availability: Jun-2019

Compiler Version Notes (Continued)

Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
C++ | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
    | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
==============================================================================
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
C++ | 523.xalancbmk_r(peak)
==============================================================================
Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
C++ | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
    | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
==============================================================================
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
Fortran | 548.exchange2_r(base, peak)
==============================================================================
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

(Continued on next page)
**SPEC CPU®2017 Integer Rate Result**

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Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL360 Gen10
(2.40 GHz, Intel Xeon Silver 4210R)

**SPECrate®2017_int_base = 114**

**SPECrate®2017_int_peak = 119**

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<th>CPU2017 License: 3</th>
<th>Test Date: Mar-2020</th>
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<td>Test Sponsor: HPE</td>
<td>Hardware Availability: Apr-2020</td>
</tr>
<tr>
<td>Tested by: HPE</td>
<td>Software Availability: Jun-2019</td>
</tr>
</tbody>
</table>

---

**Base Compiler Invocation (Continued)**

Fortran benchmarks:
ifort -m64

---

**Base Portability Flags**

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

---

**Base Optimization Flags**

C benchmarks:
-W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

C++ benchmarks:
-W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

---

**Peak Compiler Invocation**

C benchmarks (except as noted below):
icc -m64 -std=c11

(Continued on next page)
Peak Compiler Invocation (Continued)


C++ benchmarks (except as noted below):
   icpc -m64

523.xalancbmk_r: icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin

Fortran benchmarks:
   ifort -m64

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:

500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-fno-strict-overflow
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

502.gcc_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc

505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64

(Continued on next page)
**Hewlett Packard Enterprise**  
(Test Sponsor: HPE)  
ProLiant DL360 Gen10  
(2.40 GHz, Intel Xeon Silver 4210R)

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<td>SPEC CPU®2017 int_peak = 119</td>
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**CPU2017 License:** 3  
**Test Sponsor:** HPE  
**Tested by:** HPE  
**Test Date:** Mar-2020  
**Hardware Availability:** Apr-2020  
**Software Availability:** Jun-2019

### Peak Optimization Flags (Continued)

505.mcf_r (continued):  
- lqkmalloc

525.x264_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -03 -no-prec-div  
- qopt-mem-layout-trans=4 -fno-alias  
- L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
- lqkmalloc

557.xz_r: Same as 505.mcf_r

C++ benchmarks:

520.omnetpp_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -03 -no-prec-div  
- qopt-mem-layout-trans=4  
- L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
- lqkmalloc

523.xalancbmk_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
- xCORE-AVX512 -03 -no-prec-div -qopt-mem-layout-trans=4  
- L/usr/local/je5.0.1-32/lib -ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -03 -no-prec-div  
- qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte  
- L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
- lqkmalloc

The flags files that were used to format this result can be browsed at:

- [http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.html](http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.html)

You can also download the XML flags sources by saving the following links:

- [http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.xml](http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.xml)

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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