Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6246R, 3.40GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECspeed®2017_fp_base = 145
SPECspeed®2017_fp_peak = 146

Threads

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SPECspeed®2017_fp_base (145)  SPECspeed®2017_fp_peak (146)

Hardware
CPU Name: Intel Xeon Gold 6246R
Max MHz: 4100
Nominal: 3400
Enabled: 32 cores, 2 chips
Orderable: 1.2 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 35.75 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
Storage: 1 x 240 GB SSD SAS
Other: None

Software
OS: SUSE Linux Enterprise Server 15 (x86_64)
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
Parallel: Yes
Firmware: Version 4.0.4b released Apr-2019
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: None
Power Management: BIOS set to prefer performance at the cost of additional power usage
SPEC CPU®2017 Floating Point Speed Result

Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6246R, 3.40GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Apr-2020
Hardware Availability: Feb-2020
Tested by: Cisco Systems
Software Availability: May-2019

Results Table

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</table>

SPECspeed®2017_fp_base = 145
SPECspeed®2017_fp_peak = 146

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6246R, 3.40GHz)

SPEC CPU®2017 Floating Point Speed Result
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SPECspeed®2017_fp_base = 145
SPECspeed®2017_fp_peak = 146

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
SNC set to Disabled
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7ed21e6e46a485a0011
running on linux-1t71 Sun Apr 12 19:13:49 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name: Intel(R) Xeon(R) Gold 6246R CPU @ 3.40GHz
  2 "physical id"s (chips)
  32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
siblings : 16
physical 0: cores 0 2 3 6 8 12 13 17 18 19 20 21 24 26 27 29
physical 1: cores 0 1 2 3 5 6 8 9 12 13 18 19 21 26 27 29

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 32
On-line CPU(s) list: 0-31
Thread(s) per core: 1
Core(s) per socket: 16
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6246R CPU @ 3.40GHz
Stepping: 7
CPU MHz: 3400.000
CPU max MHz: 4100.0000
CPU min MHz: 1200.0000
BogoMIPS: 6800.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6246R, 3.40GHz)

| SPECspeed®2017_fp_base = 145 |
| SPECspeed®2017_fp_peak = 146 |

Platform Notes (Continued)

L2 cache: 1024K
L3 cache: 36608K
NUMA node0 CPU(s): 0-15
NUMA node1 CPU(s): 16-31
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmperf tsc_known_freq pni pmlu dq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdmg fma cx16 xtpre pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_13 cdp_13 invpcid_single intel_pmm mba tpr_shadow vni flexpriority ept
vpid fsgsbase tsc_adjust bm1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rd_t_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsaves cx8env xi tbe stray qm llc qm_occup llc qm_mb_total qm_mb_local
lbpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_request_ku
ospke avx512_vnni arch_capabilities ssbd

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.

available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
node 0 size: 385429 MB
node 0 free: 384758 MB
node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
node 1 size: 387045 MB
node 1 free: 379586 MB
node distances:
node 0 1
 0: 10 21
 1: 21 10

From /proc/meminfo

MemTotal: 791014136 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*

os-release:

NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6246R, 3.40GHz)  

**SPEC CPU®2017 Floating Point Speed Result**

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<th>CPU2017 License: 9019</th>
<th>Test Date: Apr-2020</th>
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<td>Test Sponsor: Cisco Systems</td>
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<td>Software Availability: May-2019</td>
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**SPECspeed®2017_fp_base = 145**

**SPECspeed®2017_fp_peak = 146**

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**Platform Notes (Continued)**

```
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
    Linux linux-lt71 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-3620 (L1 Terminal Fault):        No status reported
Microarchitectural Data Sampling:            No status reported
CVE-2017-5754 (Meltdown):                  Not affected
CVE-2018-3639 (Speculative Store Bypass):  Mitigation: Speculative Store Bypass disabled
                               via prctl and seccomp
CVE-2017-5753 (Spectre variant 1):         Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2):         Mitigation: Indirect Branch Restricted
                               Speculation, IBPB, IBRS_FW

run-level 3 Apr 12 14:49

SPEC is set to: /home/cpu2017
    Filesystem     Type   Size  Used Avail Use% Mounted on
    /dev/sdb1      btrfs  224G   13G  211G   6% /home

From /sys/devices/virtual/dmi/id
    BIOS:    Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
    Vendor:  Cisco Systems Inc
    Product: UCSB-B200-M5
    Serial:  FCH221572HW

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
    Memory: 24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)
```

---

**Compiler Version Notes**

```
==============================================================================
C               | 619.lbm_s(base, peak) 638.imagick_s(base, peak)
| 644.nab_s(base, peak)
------------------------------------------------------------------------------
```

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64

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Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6246R, 3.40GHz)

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SPEC CPU 2017 Floating Point Speed Result

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Cisco UCS B200 M5 (Intel Xeon Gold 6246R, 3.40GHz)

Compiler Version Notes (Continued)

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Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

(Continued on next page)
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Base Compiler Invocation (Continued)

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6246R, 3.40GHz)  

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CPU2017 License: 9019  
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Tested by: Cisco Systems

Test Date: Apr-2020  
Hardware Availability: Feb-2020  
Software Availability: May-2019

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
603.bwaves_s: -prof-gen(pass 1) -prof-use(pass 2) -DSPEC_SUPPRESS_OPENMP  
-DSPEC_OPENMP -O2 -xCORE-AVX512 -qopt-prefetch -ipo -O3  
-ffinite-math-only -no-prec-div -qopt-mem-layout-trans=4  
-qopenmp -nostandard-realloc-lhs

649.fotonik3d_s: Same as 603.bwaves_s

654.roms_s: -DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4  
-qopenmp -nostandard-realloc-lhs

Benchmarks using both Fortran and C:
621.wrf_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512  
-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div  
-qopt-mem-layout-trans=4 -DSPEC_SUPPRESS_OPENMP -qopenmp  
-DSPEC_OPENMP -nostandard-realloc-lhs

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6246R, 3.40GHz)

SPECspeed®2017_fp_base = 145
SPECspeed®2017_fp_peak = 146

Peak Optimization Flags (Continued)

627.cam4_s: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-DSPEC_OPENMP -nostandard-realloc-lhs

628.pop2_s: Same as 621.wrf_s

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revK.xml