## SPEC CPU®2017 Integer Rate Result

**Dell Inc.**

PowerEdge T440 (Intel Xeon Silver 4214R, 2.40 GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>156</td>
<td>162</td>
</tr>
</tbody>
</table>

### Hardware

- **CPU Name:** Intel Xeon Silver 4214R
- **Max MHz:** 3500
- **Nominal:** 2400
- **Enabled:** 24 cores, 2 chips, 2 threads/core
- **Orderable:** 1.2 chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 16.5 MB I+D on chip per chip
- **Memory:** 384 GB (12 x 32 GB 2Rx8 PC4-2933V-R, running at 2933)
- **Storage:** 1 x 1.92 TB SATA SSD
- **Other:** None

### Software

- **OS:** Red Hat Enterprise Linux 8.1
- **Compiler:** C/C++: Version 19.1.1.217 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.1.1.217 of Intel Fortran Compiler for Linux
- **Parallel:** No
- **Firmware:** Version 2.7.7 released May-2020
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 32/64-bit
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage

---

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<th>Benchmark</th>
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<th>SPECrate®2017_int_base</th>
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<td>Nominal:</td>
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## Results Table

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### Compiler Notes

The inconsistent Compiler version information under Compiler Version section is due to a discrepancy in Intel Compiler. The correct version of C/C++ compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux. The correct version of Fortran compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux.

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH = "'/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/jc5.0.1-32"
MALLOCONF = "retain:true"
```
## General Notes

Binaries compiled on a system with 1x Intel Core i9-9900K CPU + 64GB RAM
memory using Redhat Enterprise Linux 8.0
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
umactl --interleave=all runcpu <etc>
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

## Platform Notes

BIOS settings:
Sub NUMA Cluster enabled
Virtualization Technology disabled
System Profile set to Custom
CPU Performance set to Maximum Performance
C States set to Autonomous
C1E disabled
Uncore Frequency set to Dynamic
Energy Efficiency Policy set to Performance
Memory Patrol Scrub disabled
Logical Processor enabled
CPU Interconect Bus Link Power Management disabled
PCI ASPM L1 Link Power Management disabled
UPI Prefetch enabled
LLC Prefetch disabled
Dead Line LLC Alloc enabled
Directory AtoS disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7ed1be6e46a485a0011
running on localhost.localdomain Wed May 20 00:01:16 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

(Continued on next page)
Dell Inc.

PowerEdge T440 (Intel Xeon Silver 4214R, 2.40 GHz)

CPU2017 License: 55  Test Date: Apr-2020
Test Sponsor: Dell Inc.  Hardware Availability: Feb-2020
Tested by: Dell Inc.  Software Availability: Apr-2020

Platform Notes (Continued)

From /proc/cpuinfo

    model name : Intel(R) Xeon(R) Silver 4214R CPU @ 2.40GHz
    2 "physical id"s (chips)
    48 "processors"
    cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
    cpu cores : 12
    siblings : 24
    physical 0: cores 0 1 2 3 4 5 8 9 10 11 12 13
    physical 1: cores 0 1 2 3 4 5 8 9 10 11 12 13

From lscpu:
    Architecture: x86_64
    CPU op-mode(s): 32-bit, 64-bit
    Byte Order: Little Endian
    CPU(s): 48
    On-line CPU(s) list: 0-47
    Thread(s) per core: 2
    Core(s) per socket: 12
    Socket(s): 2
    NUMA node(s): 4
    Vendor ID: GenuineIntel
    CPU family: 6
    Model: 85
    Model name: Intel(R) Xeon(R) Silver 4214R CPU @ 2.40GHz
    Stepping: 7
    CPU MHz: 3151.111
    CPU max MHz: 3500.0000
    CPU min MHz: 1000.0000
    BogoMIPS: 4800.00
    Virtualization: VT-x
    L1d cache: 32K
    L1i cache: 32K
    L2 cache: 1024K
    L3 cache: 16896K
    NUMA node0 CPU(s): 0,4,8,12,16,20,24,28,32,36,40,44
    NUMA node1 CPU(s): 1,5,9,13,17,21,25,29,33,37,41,45
    NUMA node2 CPU(s): 2,6,10,14,18,22,26,30,34,38,42,46
    NUMA node3 CPU(s): 3,7,11,15,19,23,27,31,35,39,43,47
    Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_pni ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vtcesr vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 irds invpcid rtm
# Dell Inc. PowerEdge T440 (Intel Xeon Silver 4214R, 2.40 GHz)

<table>
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<tr>
<th>SPEC CPU®2017 License</th>
<th>Test Date</th>
<th>Hardware Availability</th>
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<tr>
<td>55</td>
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<tr>
<th>SPECrate®2017_int_base</th>
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<tr>
<td>156</td>
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<tbody>
<tr>
<td>162</td>
</tr>
</tbody>
</table>

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## Platform Notes (Continued)

```plaintext
cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsavc xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local dtherm ida arat pln pts pku ospke avx512_vnni md_clear flush_l1d arch_capabilities
```

/proc/cpuinfo cache data

```plaintext
cache size : 16896 KB
```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```plaintext
available: 4 nodes (0-3)
node 0 cpus: 0 4 8 12 16 20 24 28 32 36 40 44
node 0 size: 95307 MB
node 0 free: 90692 MB
node 1 cpus: 1 5 9 13 17 21 25 29 33 37 41 45
node 1 size: 96739 MB
node 1 free: 96360 MB
node 2 cpus: 2 6 10 14 18 22 26 30 34 38 42 46
node 2 size: 96765 MB
node 2 free: 95144 MB
node 3 cpus: 3 7 11 15 19 23 27 31 35 39 43 47
node 3 size: 96764 MB
node 3 free: 95865 MB
node distances:

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<th>3</th>
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<tr>
<td>3</td>
<td>21</td>
<td>11</td>
<td>21</td>
<td>10</td>
</tr>
</tbody>
</table>
```

From /proc/meminfo

```plaintext
MemTotal: 394831636 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
```

From /etc/*release* /etc/*version*

```plaintext
os-release:
  NAME="Red Hat Enterprise Linux"
  VERSION="8.1 (Ootpa)"
  ID="rhel"
  ID_LIKE="fedora"
  VERSION_ID="8.1"
  PLATFORM_ID="platform:el8"
  PRETTY_NAME="Red Hat Enterprise Linux 8.1 (Ootpa)"
  ANSI_COLOR="0;31"
redhat-release: Red Hat Enterprise Linux release 8.1 (Ootpa)
system-release: Red Hat Enterprise Linux release 8.1 (Ootpa)
```
SPEC CPU®2017 Integer Rate Result

Dell Inc.

PowerEdge T440 (Intel Xeon Silver 4214R, 2.40 GHz)

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<tr>
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CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

Test Date: Apr-2020
Hardware Availability: Feb-2020
Software Availability: Apr-2020

Platforms Notes (Continued)

```
uname -a:
Linux localhost.localdomain 4.18.0-147.el8.x86_64 #1 SMP Thu Sep 26 15:52:44 UTC 2019
x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

- CVE-2018-3620 (L1 Terminal Fault): Not affected
- Microarchitectural Data Sampling: Not affected
- CVE-2017-5754 (Meltdown): Not affected
- CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
- CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs barriers and __user pointer sanitization
- CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

run-level 3 May 19 23:54 last=5

SPEC is set to: /home/cpu2017
```
Filesystem          Type  Size  Used Avail Use% Mounted on
/dev/mapper/rhel-home xfs   1.7T   28G  1.7T   2% /home
```

From /sys/devices/virtual/dmi/id
BIOS: Dell Inc. 2.7.7 05/06/2020
Vendor: Dell Inc.
Product: PowerEdge T440
Product Family: PowerEdge
Serial: FBLH613

```
Memory:
  4x 00AD00B300AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933
  8x 00AD063200AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933
  4x Not Specified Not Specified
```

(End of data from sysinfo program)

Compiler Version Notes

```
C       | 502.gcc_r(peak)
```

(Continued on next page)
## SPEC CPU®2017 Integer Rate Result

### Dell Inc.

**PowerEdge T440 (Intel Xeon Silver 4214R, 2.40 GHz)**

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**SPECrate®2017_int_base = 156**

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### Compiler Version Notes (Continued)

| Intel(R) C Compiler for applications running on IA-32, Version 2021.1 NextGen Build 20200304 |
| Copyright (C) 1985-2020 Intel Corporation. All rights reserved. |

| C | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak) |
|   | 525.x264_r(base, peak) 557.xz_r(base) |

| Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1 NextGen Build 20200304 |
| Copyright (C) 1985-2020 Intel Corporation. All rights reserved. |

| C | 500.perlbench_r(peak) 557.xz_r(peak) |

| Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.1.1.217 Build 20200306 |
| Copyright (C) 1985-2020 Intel Corporation. All rights reserved. |

| C | 502.gcc_r(peak) |

| Intel(R) C Compiler for applications running on IA-32, Version 2021.1 NextGen Build 20200304 |
| Copyright (C) 1985-2020 Intel Corporation. All rights reserved. |

| C | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak) |
|   | 525.x264_r(base, peak) 557.xz_r(base) |

| Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1 NextGen Build 20200304 |
| Copyright (C) 1985-2020 Intel Corporation. All rights reserved. |

| C | 500.perlbench_r(peak) 557.xz_r(peak) |

| Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.1.1.217 Build 20200306 |
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### Compiler Version Notes (Continued)

```
C       | 502.gcc_r(peak)
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Intel(R) C Compiler for applications running on IA-32, Version 2021.1 NextGen
Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
        | 525.x264_r(base, peak) 557.xz_r(base)
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Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
C       | 500.perlbench_r(peak) 557.xz_r(peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
C++     | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base, peak)
        | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
Fortran | 548.exchange2_r(base, peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.1.1.217 Build 20200306
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```
## Dell Inc. PowerEdge T440 (Intel Xeon Silver 4214R, 2.40 GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base = 156</th>
<th>SPECrate®2017_int_peak = 162</th>
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<tr>
<td>CPU2017 License: 55</td>
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### Base Compiler Invocation

- C benchmarks: icc
- C++ benchmarks: icpc
- Fortran benchmarks: ifort

### Base Portability Flags

- `500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64`
- `502.gcc_r: -DSPEC_LP64`
- `505.mcf_r: -DSPEC_LP64`
- `520.omnetpp_r: -DSPEC_LP64`
- `523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX`
- `525.x264_r: -DSPEC_LP64`
- `531.deepsjeng_r: -DSPEC_LP64`
- `541.leela_r: -DSPEC_LP64`
- `548.exchange2_r: -DSPEC_LP64`
- `557.xz_r: -DSPEC_LP64`

### Base Optimization Flags

- **C benchmarks:**
  - `-m64 -qnextgen -std=c11`
  - `-Wl, -plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs`
  - `-xCORE-AVX2 -O3 -ffast-math -f1to -mfpmath=sse -funroll-loops`
  - `-fuse-ld=gold -qopt-mem-layout-trans=4`
  - `-l/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin -lqkmalloc`

- **C++ benchmarks:**
  - `-m64 -qnextgen -Wl,-plugin-opt=-x86-branches-within-32B-boundaries`
  - `-Wl,-z,muldefs -xCORE-AVX2 -O3 -ffast-math -f1to -mfpmath=sse`
  - `-funroll-loops -fuse-ld=gold -qopt-mem-layout-trans=4`
  - `-l/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin -lqkmalloc`

- **Fortran benchmarks:**
  - `-m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs`
  - `-xCORE-AVX2 -O3 -ipo -no-prec-div -qopt-mem-layout-trans=4`

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Dell Inc.

PowerEdge T440 (Intel Xeon Silver 4214R, 2.40 GHz)

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Base Optimization Flags (Continued)

Fortran benchmarks (continued):
-nostandard-realloc-lhs -align array32byte -auto
-mbranches-within-32B-boundaries
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-lqkmalloc

Peak Compiler Invocation

C benchmarks:
icc
C++ benchmarks:
icpc
Fortran benchmarks:
ifort

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:
500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)
-xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-strict-overflow
-mbranches-within-32B-boundaries
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-lqkmalloc

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SPEC CPU®2017 Integer Rate Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

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PowerEdge T440 (Intel Xeon Silver 4214R, 2.40 GHz)

| SPECrate®2017_int_base = 156 |
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Peak Optimization Flags (Continued)

502.gcc_r: -m32
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/ia32_lin
-std=gnu89
-WL,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -fprofile-generate(pass 1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX2 -flto
-O3(pass 1) -03 -ffast-math -qnextgen -fuse-ld=gold
-qopt-mem-layout-trans=4 -L/usr/local/jemalloc32-5.0.1/lib
-ljemalloc

505.mcf_r: basepeak = yes

525.x264_r: -m64 -qnextgen -std=c11
-W1,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -xCORE-AVX2 -flto -O3 -ffast-math
-fuse-ld=gold -qopt-mem-layout-trans=4 -fno-alias
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-lqkmalloc

557.xz_r: -Wl,-z,muldefs -xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-lqkmalloc

C++ benchmarks:

520.omnetpp_r: basepeak = yes

523.xalancbmk_r: basepeak = yes

531.deepsjeng_r: basepeak = yes

541.leela_r: basepeak = yes

Fortran benchmarks:

548.exchange2_r: basepeak = yes

The flags files that were used to format this result can be browsed at
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You can also download the XML flags sources by saving the following links:

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Tested with SPEC CPU®2017 v1.1.0 on 2020-05-20 01:01:15-0400.
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