## SPEC CPU®2017 Integer Rate Result

**Hewlett Packard Enterprise**  
(Test Sponsor: HPE)  
Synergy 480 Gen10  
(2.30 GHz, Intel Xeon Gold 6252N)

<table>
<thead>
<tr>
<th></th>
<th>SPECrate®2017_int_base = 262</th>
<th>SPECrate®2017_int_peak = 272</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU2017 License:</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>Test Sponsor:</td>
<td>HPE</td>
<td></td>
</tr>
<tr>
<td>Tested by:</td>
<td>HPE</td>
<td></td>
</tr>
<tr>
<td>CPU Name:</td>
<td>Intel Xeon Gold 6252N</td>
<td></td>
</tr>
<tr>
<td>Max MHz:</td>
<td>3600</td>
<td></td>
</tr>
<tr>
<td>Nominal:</td>
<td>2300</td>
<td></td>
</tr>
<tr>
<td>Enabled:</td>
<td>48 cores, 2 chips, 2 threads/core</td>
<td></td>
</tr>
<tr>
<td>Orderable:</td>
<td>1, 2 chip(s)</td>
<td></td>
</tr>
<tr>
<td>Cache L1:</td>
<td>32 KB I + 32 KB D on chip per core</td>
<td></td>
</tr>
<tr>
<td>L2:</td>
<td>1 MB I+D on chip per core</td>
<td></td>
</tr>
<tr>
<td>L3:</td>
<td>35.75 MB I+D on chip per chip</td>
<td></td>
</tr>
<tr>
<td>Other:</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>Memory:</td>
<td>384 GB (24 x 16 GB 2Rx8 PC4-2933Y-R)</td>
<td></td>
</tr>
<tr>
<td>Storage:</td>
<td>1 x 400 GB SAS SSD, RAID 0</td>
<td></td>
</tr>
<tr>
<td>Other:</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>OS:</td>
<td>SUSE Linux Enterprise Server 15 SP1 (x86_64)</td>
<td></td>
</tr>
<tr>
<td>Compiler:</td>
<td>C/C++: Version 19.0.4.227 of Intel C/C++ Compiler Build 20190416 for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler Build 20190416 for Linux;</td>
<td></td>
</tr>
<tr>
<td>Parallel:</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>Firmware:</td>
<td>HPE BIOS Version 142 v2.22 (11/13/2019) released Nov-2019</td>
<td></td>
</tr>
<tr>
<td>System State:</td>
<td>Run level 3 (multi-user)</td>
<td></td>
</tr>
<tr>
<td>Base Pointers:</td>
<td>64-bit</td>
<td></td>
</tr>
<tr>
<td>Peak Pointers:</td>
<td>32/64-bit</td>
<td></td>
</tr>
<tr>
<td>Other:</td>
<td>jemalloc memory allocator V5.0.1</td>
<td></td>
</tr>
<tr>
<td>Power Management:</td>
<td>BIOS set to prefer performance at the cost of additional power usage</td>
<td></td>
</tr>
</tbody>
</table>

### SPEC CPU®2017 Integer Rate Result

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
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<tbody>
<tr>
<td>perlbench_r</td>
<td>96</td>
<td>252</td>
<td>272</td>
</tr>
<tr>
<td>gcc_r</td>
<td>96</td>
<td>216</td>
<td>231</td>
</tr>
<tr>
<td>mcf_r</td>
<td>96</td>
<td>174</td>
<td>174</td>
</tr>
<tr>
<td>omnetpp_r</td>
<td>96</td>
<td>174</td>
<td>174</td>
</tr>
<tr>
<td>xalancbmk_r</td>
<td>96</td>
<td>281</td>
<td>304</td>
</tr>
<tr>
<td>x264_r</td>
<td>96</td>
<td>550</td>
<td>574</td>
</tr>
<tr>
<td>deepsjeng_r</td>
<td>96</td>
<td>220</td>
<td>230</td>
</tr>
<tr>
<td>leela_r</td>
<td>96</td>
<td>209</td>
<td>208</td>
</tr>
<tr>
<td>exchange2_r</td>
<td>96</td>
<td>519</td>
<td>518</td>
</tr>
<tr>
<td>xz_r</td>
<td>96</td>
<td>173</td>
<td>173</td>
</tr>
</tbody>
</table>

**Notes:**  
- SPEC Rate® 2017 (International):  
- SPEC Rate® 2017 (International) is a benchmark suite for measuring the integer rate performance of computers.  
- The results are expressed in terms of SPECmark, which is a normalized score.  
- The test sponsors and the hardware details are provided in the table above.  
- The benchmarks included in the test are Perlbench, GCC, Mcf, Omnet++ and Xalancbmk, X264, DeepSjeng, Leela, Exchange2, and Xz.  
- The results include the number of copies run for each benchmark and the SPECmark scores for both peak and base performance.
SPEC CPU®2017 Integer Rate Result
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SPECrate®2017_int_base = 262
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Results Table

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<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
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<tbody>
<tr>
<td>500.perlbench_r</td>
<td>96</td>
<td>791</td>
<td>193</td>
<td>790</td>
<td>194</td>
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<td>688</td>
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<tr>
<td>502.gcc_r</td>
<td>96</td>
<td>626</td>
<td>217</td>
<td>634</td>
<td>215</td>
<td>629</td>
<td>216</td>
<td>96</td>
<td>543</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>96</td>
<td>475</td>
<td>326</td>
<td>477</td>
<td>325</td>
<td>478</td>
<td>325</td>
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<tr>
<td>520.omnetpp_r</td>
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<td>725</td>
<td>174</td>
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<td>726</td>
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<tr>
<td>523.xalancbmk_r</td>
<td>96</td>
<td>363</td>
<td>279</td>
<td>361</td>
<td>281</td>
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<tr>
<td>525.x264_r</td>
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<td>549</td>
<td>305</td>
<td>550</td>
<td>302</td>
<td>556</td>
<td>96</td>
<td>293</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>96</td>
<td>500</td>
<td>220</td>
<td>500</td>
<td>220</td>
<td>500</td>
<td>220</td>
<td>96</td>
<td>500</td>
</tr>
<tr>
<td>541.leela_r</td>
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<td>761</td>
<td>209</td>
<td>764</td>
<td>208</td>
<td>757</td>
<td>210</td>
<td>96</td>
<td>764</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>96</td>
<td>485</td>
<td>519</td>
<td>486</td>
<td>518</td>
<td>485</td>
<td>519</td>
<td>96</td>
<td>485</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>96</td>
<td>600</td>
<td>173</td>
<td>600</td>
<td>173</td>
<td>599</td>
<td>173</td>
<td>96</td>
<td>600</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with: jema
sync; echo 3 > /proc/sys/vm/drop_caches

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017_u4/lib/intel64:/home/cpu2017_u4/lib/ia32:/home/cpu2017_u4/jem5.0.1-32"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)

(Continued on next page)
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CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

General Notes (Continued)

is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Configuration:
Thermal Configuration set to Maximum Cooling
Memory Patrol Scrubbing set to Disabled
LLC Prefetch set to Enabled
LLC Dead Line Allocation set to Disabled
Enhanced Processor Performance set to Enabled
Workload Profile set to General Throughput Compute
Workload Profile set to Custom
Energy/Performance Bias set to Balanced Performance

Sysinfo program /home/cpu2017_u4/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edbd1e6e46a485a0011
running on sy480-sys2 Sat May 30 08:08:58 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6252N CPU @ 2.30GHz
  2 "physical id"s (chips)
  96 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 24
siblings : 48
physical 0: cores 0 1 2 3 4 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29
physical 1: cores 0 1 2 3 4 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 48 bits virtual
CPU(s): 96

(Continued on next page)
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CPU2017 License: 3
Test Sponsor: HPE
Test Date: May-2020
Hardware Availability: Nov-2019
Tested by: HPE
Software Availability: Jun-2019

Platform Notes (Continued)

On-line CPU(s) list: 0-95
Thread(s) per core: 2
Core(s) per socket: 24
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6252N CPU @ 2.30GHz
Stepping: 7
CPU MHz: 2300.000
BogoMIPS: 4600.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 36608K
NUMA node0 CPU(s): 0-11,48-59
NUMA node1 CPU(s): 12-23,60-71
NUMA node2 CPU(s): 24-35,72-83
NUMA node3 CPU(s): 36-47,84-95
Flags:

fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtrr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 cdp_13
invpcid_single intel_pmm ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi
flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm
cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd
avx512bw avx512vl xsaveopt xsaves xsavec xgetbv1 xsavec cqm_llc cqm_occupa llc
qm_mbb_total
cqm_mbb_local dl therm ida arat pln pts pk uospke avx512_vnni md_clear flush_lld
arch_capabilities

/proc/cpuinfo cache data
cache size: 36608 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.

available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 48 49 50 51 52 53 54 55 56 57 58 59
node 0 size: 96285 MB
node 0 free: 95820 MB
node 1 cpus: 12 13 14 15 16 17 18 19 20 21 22 23 60 61 62 63 64 65 66 67 68 69 70 71
node 1 size: 96763 MB
node 1 free: 96483 MB
node 2 cpus: 24 25 26 27 28 29 30 31 32 33 34 35 72 73 74 75 76 77 78 79 80 81 82 83

(Continued on next page)
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Platform Notes (Continued)

node 2 size: 96733 MB  
node 2 free: 96528 MB  
node 3 cpus: 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59  
node 3 size: 96564 MB  
node 3 free: 96325 MB  
node distances:  
node 0 1 2 3  
0: 10 21 31 31  
1: 21 10 31 31  
2: 31 31 10 21  
3: 31 31 21 10

From /proc/meminfo  
MemTotal: 395620352 kB  
HugePages_Total: 0  
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*  
os-release:  
NAME="SLES"  
VERSION="15-SP1"  
VERSION_ID="15.1"  
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP1"  
ID="sles"  
ID_LIKE="suse"  
ANSI_COLOR="0;32"  
CPE_NAME="cpe:/o:suse:sles:15:sp1"

uname -a:  
Linux sy480-sys2 4.12.14-195-default #1 SMP Tue May 7 10:55:11 UTC 2019 (8fba516)  
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): Not affected  
Microarchitectural Data Sampling: Not affected  
CVE-2017-5754 (Meltdown): Not affected  
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp  
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization  
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

run-level 3 May 30 08:06

SPEC is set to: /home/cpu2017_u4

Filesystem Type Size Used Avail Use% Mounted on

(Continued on next page)
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Test Date: May-2020
Hardware Availability: Nov-2019
Software Availability: Jun-2019

Platform Notes (Continued)
/dev/sda2     btrfs  371G  131G  240G  36% /home

From /sys/devices/virtual/dmi/id
BIOS:     HPE I42 11/13/2019
Vendor:   HPE
Product:  Synergy 480 Gen10
Product Family: Synergy
Serial:   MXQ72204FC

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
24x UNKNOWN NOT AVAILABLE 16 GB 2 rank 2933

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C       | 502.gcc_r(peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C       | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
       | 525.x264_r(base, peak) 557.xz_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C       | 502.gcc_r(peak)
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version
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<td>Software Availability: Jun-2019</td>
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</tbody>
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**SPECrate®2017_int_base = 262**  
**SPECrate®2017_int_peak = 272**

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**Compiler Version Notes (Continued)**

```plaintext
C        | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)  
          | 525.x264_r(base, peak) 557.xz_r(base, peak)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
```

---

```plaintext
C++     | 523.xalancbmk_r(peak)
```

Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version  
19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---

```plaintext
C++     | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)  
          | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
```

---

```plaintext
C++     | 523.xalancbmk_r(peak)
```

Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version  
19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---

```plaintext
C++     | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)  
          | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
```

---

```plaintext
Fortran | 548.exchange2_r(base, peak)
```

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.0.4.227 Build 20190416
```

(Continued on next page)
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Compiler Version Notes (Continued)
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Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-1qkmalloc

C++ benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-1qkmalloc

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CPU2017 License: 3
Tested by: HPE

Base Optimization Flags (Continued)

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m64 -std=c11


C++ benchmarks (except as noted below):
icpc -m64

523.xalancbmk_r: icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin

Fortran benchmarks:
ifort -m64

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:
500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

Hewlett Packard Enterprise
(Test Sponsor: HPE)
Synergy 480 Gen10
(2.30 GHz, Intel Xeon Gold 6252N)

SPECrate®2017_int_base = 262
SPECrate®2017_int_peak = 272

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Test Date: May-2020
Hardware Availability: Nov-2019
Software Availability: Jun-2019

Peak Optimization Flags (Continued)

500.perlbench_r (continued):
- fno-strict-overflow 
- L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64 
- lqkmalloc

502.gcc_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo 
- xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4 
- L/usr/local/je5.0.1-32/lib -ljemalloc

505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div 
- qopt-mem-layout-trans=4 
- L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64 
- lqkmalloc

525.x264_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div 
- qopt-mem-layout-trans=4 -fno-alias 
- L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64 
- lqkmalloc

557.xz_r: Same as 505.mcf_r

C++ benchmarks:

520.omnetpp_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div 
- qopt-mem-layout-trans=4 
- L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64 
- lqkmalloc

523.xalancbmk_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo 
- xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4 
- L/usr/local/je5.0.1-32/lib -ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:
- Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div 
- qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte 
- L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64 
- lqkmalloc

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.html
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You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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