Lenovo Global Technology
ThinkSystem SR650
(2.40 GHz, Intel Xeon Silver 4214R)

SPECraten®2017_fp_base =  157
SPECraten®2017_fp_peak = Not Run

CPU2017 License: 9017
Test Sponsor: Lenovo Global Technology
Tested by: Lenovo Global Technology
Test Date: Jul-2020
Hardware Availability: Mar-2020
Software Availability: Apr-2020

Copies

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<tr>
<td>554.roms_r</td>
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</table>

Hardware

CPU Name: Intel Xeon Silver 4214R
Max MHz: 3500
Nominal: 2400
Enabled: 24 cores, 2 chips, 2 threads/core
Orderable: 1,2 chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 16.5 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933Y-R, running at 2400)
Storage: 1 x 800 GB SATA SSD
Other: None

Software

OS: SUSE Linux Enterprise Server 15 SP1 (x86_64)
Compiler: C/C++: Version 19.1.1.217 of Intel
Compiler: Fortran: Version 19.1.1.217 of Intel Fortran
Parallel: No
Firmware: Lenovo BIOS Version IVE155L 2.61 released May-2020
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS set to prefer performance at the cost of additional power usage
Lenovo Global Technology
ThinkSystem SR650
(2.40 GHz, Intel Xeon Silver 4214R)

CPU2017 License: 9017
Test Sponsor: Lenovo Global Technology
Tested by: Lenovo Global Technology

Results Table

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Compiler Notes
The inconsistent Compiler version information under Compiler Version section is due to a discrepancy in Intel Compiler.
The correct version of C/C++ compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux
The correct version of Fortran compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.
For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = 
"/home/cpu2017-1.1.0-ic19.1.1/lib/intel64:/home/cpu2017-1.1.0-ic19.1.1/j
e5.0.1-64"

MALLOC_CONF = "retain:true"
Lenovo Global Technology
ThinkSystem SR650
(2.40 GHz, Intel Xeon Silver 4214R)

SPECrate®2017_fp_base = 157
SPECrate®2017_fp_peak = Not Run

General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM memory using Redhat Enterprise Linux 8.0
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.: numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS configuration:
Choose Operating Mode set to Maximum Performance and then set it to Custom Mode
C-States set to Legacy

Sysinfo program /home/cpu2017-1.1.0-ic19.1.1/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7ed1e6e46a485a0011 running on linux-xpyz Tue Jul 14 18:11:08 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4214R CPU @ 2.40GHz
  2 "physical id"s (chips)
  48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 12
siblings : 24
physical 0: cores 0 1 2 3 4 5 8 9 10 11 12 13
physical 1: cores 0 1 2 3 4 5 8 9 10 11 12 13

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit

(Continued on next page)
Lenovo Global Technology
ThinkSystem SR650
(2.40 GHz, Intel Xeon Silver 4214R)
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SPECrater®2017_fp_base = 157
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CPU2017 License: 9017
Test Sponsor: Lenovo Global Technology
Tested by: Lenovo Global Technology

Platform Notes (Continued)

node 1 size: 387036 MB
node 1 free: 386630 MB
node distances:
node  0  1
0:  10  21
1:  21  10

From /proc/meminfo
MemTotal:       792293660 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15-SP1"
VERSION_ID="15.1"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP1"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp1"

uname -a:
Linux linux-xpyz 4.12.14-195-default #1 SMP Tue May 7 10:55:11 UTC 2019 (8fba516)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

run-level 3 Jul 14 18:09

SPEC is set to: /home/cpu2017-1.1.0-ic19.1.1
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda3 xfs 737G 63G 675G 9% /

From /sys/devices/virtual/dmi/id
BIOS: Lenovo -[IVE155L-2.61]- 05/20/2020
Vendor: Lenovo

(Continued on next page)
**SPEC CPU®2017 Floating Point Rate Result**  
Copyright 2017-2020 Standard Performance Evaluation Corporation

<table>
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**CPU2017 License:** 9017  
**Test Sponsor:** Lenovo Global Technology  
**Tested by:** Lenovo Global Technology

---

**Platform Notes (Continued)**

- **Product:** ThinkSystem SR650 -[7X05RCZ000]-.  
- **Product Family:** ThinkSystem  
- **Serial:** 1234567890

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

**Memory:**
- 24x Samsung M393A4K40CB2-CVF 32 GB 2 rank 2933

(End of data from sysinfo program)

Memory on this system run at 2400 MHz due to CPU limitation.

---

**Compiler Version Notes**

```
C | 519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)  
---
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1  
NextGen Build 20200304  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

---

C++ | 508.namd_r(base) 510.parest_r(base)  
---
Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1  
NextGen Build 20200304  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

---

C++, C | 511.povray_r(base) 526.blender_r(base)  
---
Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1  
NextGen Build 20200304  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

---

C++, C, Fortran | 507.cactusBSSN_r(base)  
---
```

(Continued on next page)
Lenovo Global Technology
ThinkSystem SR650
(2.40 GHz, Intel Xeon Silver 4214R)

SPECrater®2017_fp_base = 157

SPECrater®2017_fp_peak = Not Run

CPU2017 License: 9017
Test Sponsor: Lenovo Global Technology
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Test Date: Jul-2020
Hardware Availability: Mar-2020
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Compiler Version Notes (Continued)

Intel (R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Intel (R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Intel (R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using both C and C++:
icpc icc

(Continued on next page)
Lenovo Global Technology
ThinkSystem SR650
(2.40 GHz, Intel Xeon Silver 4214R)

SPECrate®2017_fp_base = 157
SPECrate®2017_fp_peak = Not Run

Base Compiler Invocation (Continued)

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-m64 -mnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

C++ benchmarks:
-m64 -mnextgen -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Fortran benchmarks:
-m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-auto -mbranches-within-32B-boundaries

(Continued on next page)
Base Optimization Flags (Continued)

Fortran benchmarks (continued):
-\(L/usr/local/jemalloc64-5.0.1/lib -ljemalloc\)

Benchmarks using both Fortran and C:
-\(-m64 -qnextgen -std=c11\)
-\(-Wl,-plugin-opt=-x86-braches-within-32B-boundaries -Wl,-z,muldefs\)
-\(-fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse\)
-\(-funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div\)
-\(-qopt-prefetch -ffinite-math-only\)
-\(-qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs\)
-\(-align array32byte -auto -mbranches-within-32B-boundaries\)
-\(-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc\)

Benchmarks using both C and C++:
-\(-m64 -qnextgen -std=c11\)
-\(-Wl,-plugin-opt=-x86-braches-within-32B-boundaries -Wl,-z,muldefs\)
-\(-fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse\)
-\(-funroll-loops -qopt-mem-layout-trans=4\)
-\(-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc\)

Benchmarks using Fortran, C, and C++:
-\(-m64 -qnextgen -std=c11\)
-\(-Wl,-plugin-opt=-x86-braches-within-32B-boundaries -Wl,-z,muldefs\)
-\(-fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse\)
-\(-funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div\)
-\(-qopt-prefetch -ffinite-math-only\)
-\(-qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs\)
-\(-align array32byte -auto -mbranches-within-32B-boundaries\)
-\(-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc\)

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Lenovo-Platform-SPECcpu2017-Flags-V1.2-CLX-I.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Lenovo-Platform-SPECcpu2017-Flags-V1.2-CLX-I.xml

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