### SPEC CPU®2017 Integer Rate Result

<table>
<thead>
<tr>
<th>Test Sponsor: Netweb Pte Ltd</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Tyron Camarero DS400TG-48R</strong></td>
</tr>
<tr>
<td>(2.10 GHz, Intel Xeon Gold 5218R)</td>
</tr>
</tbody>
</table>

**SPECrate®2017_int_base = 227**

**SPECrate®2017_int_peak = 236**

**CPU2017 License:** 006042

**Test Date:** Jan-2021

**Test Sponsor:** Netweb Pte Ltd

**Hardware Availability:** Aug-2020

**Tested by:** Tyrone Systems

**Software Availability:** Dec-2020

---

<table>
<thead>
<tr>
<th><strong>Copies</strong></th>
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</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
</tr>
<tr>
<td>80</td>
</tr>
<tr>
<td>141</td>
</tr>
<tr>
<td>SPECrate®2017_int_base (227)</td>
</tr>
</tbody>
</table>

---

### Hardware

- **CPU Name:** Intel Xeon Gold 5218R
- **Max MHz:** 4000
- **Nominal:** 2100
- **Enabled:** 40 cores, 2 chips, 2 threads/core
- **Orderable:** 1.2 (chip)s
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 27.5 MB I+D on chip per chip
- **Other:** None
- **Memory:** 384 GB (12 x 32 GB 2Rx4 PC4-2933Y-R, running at 2666)
- **Storage:** 1 x 480 GB SATA SSD
- **Other:** None

### Software

- **OS:** CentOS Linux release 8.3.2011 4.18.0-240.el8.x86_64
- **Compiler:** C/C++: Version 19.1.1.217 of Intel C/C++ Compiler Build 20200306 for Linux; Fortran: Version 19.1.1.217 of Intel Fortran Compiler Build 20200306 for Linux
- **Parallel:** No
- **Firmware:** Version 3.3 released Feb-2020
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 32/64-bit
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage
**SPEC CPU®2017 Integer Rate Result**

**Tyrone Systems**  
(Test Sponsor: Netweb Pte Ltd)  
Tyrone Camarero DS400TG-48R  
(2.10 GHz, Intel Xeon Gold 5218R)  

**Copyright 2017-2021 Standard Performance Evaluation Corporation**

**SPECrate®2017_int_base = 227**  
**SPECrate®2017_int_peak = 236**

**Results Table**

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<thead>
<tr>
<th>Benchmark</th>
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<th>Ratio</th>
<th>Seconds</th>
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<td>712</td>
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<tr>
<td>502.gcc_r</td>
<td>80</td>
<td>629</td>
<td>180</td>
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<td>550</td>
<td>206</td>
<td>548</td>
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<td>548.exchange2_r</td>
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<td>557.xz_r</td>
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<td>613</td>
<td>141</td>
<td>612</td>
<td>141</td>
<td>612</td>
</tr>
</tbody>
</table>

**Results appear in the order in which they were run. Bold underlined text indicates a median measurement.**

**Compiler Notes**

The inconsistent Compiler version information under Compiler Version section is due to a discrepancy in Intel Compiler.  
The correct version of C/C++ compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux  
The correct version of Fortran compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

**Submit Notes**

The numaCtl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numaCtl commands to bind each copy to a specific processor.  
For details, please see the config file.

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

**Environment Variables Notes**

Environment variables set by runcpu before the start of the run:  
LD_LIBRARY_PATH = 
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"  
MALLOCONF = "retain: true"
SPEC CPU®2017 Integer Rate Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)

Tyrone Camarero DS400TG-48R
(2.10 GHz, Intel Xeon Gold 5218R)

SPEC CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

SPECrate®2017_int_base = 227
SPECrate®2017_int_peak = 236

Test Date: Jan-2021
Hardware Availability: Aug-2020
Software Availability: Dec-2020

General Notes

Binaries compiled on a system with 2x Intel Cascade Lake CPU + 384 GB RAM memory using Centos 8.2 x86_64
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
  sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
  numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation built with the Centos 8.2 x86_64, and the system compiler gcc 4.8.5 sources available from jemalloc.net or https://github.com/jemalloc/jemalloc/releases

Platform Notes

BIOS Settings:
  Power Technology = Custom
  Power Performance Tuning = BIOS Controls EPB
  ENERGY_PERF_BIAS_CFG mode = Maximum Performance
  SNC = Enable
  Stale AtoS = Disable
  IMC Interleaving = 1-way Interleave
  Patrol Scrub = Disable

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6538 of 2020-09-24 e8664e66d2d7080afeaa89d4b38e2f1c
running on localhost.localdomain Fri Jan 29 16:31:13 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
  model name : Intel(R) Xeon(R) Gold 5218R CPU @ 2.10GHz
  2 "physical id"s (chips)
  80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 20
siblings : 40
physical 0: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28

(Continued on next page)
Platform Notes (Continued)

physical 1: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 80
On-line CPU(s) list: 0-79
Thread(s) per core: 2
Core(s) per socket: 20
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 5218R CPU @ 2.10GHz
Stepping: 7
CPU MHz: 2899.952
CPU max MHz: 4000.0000
CPU min MHz: 800.0000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 28160K
NUMA node0 CPU(s): 0-2,5,6,10-12,15,16,40-42,45,46,50-52,55,56
NUMA node1 CPU(s): 3,4,7-9,13,14,17-19,43,44,47-49,53,54,57-59
NUMA node2 CPU(s): 20-22,25,26,30-32,35,36,60-62,65,66,70-72,75,76
NUMA node3 CPU(s): 23,24,27-29,33,34,37-39,63,64,67-69,73,74,77-79

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfperf pi pclmulqdq dtes64 ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm
pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c
rdond lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single
intel_pinn ssbd mba ibrs ibpb stibp ibrs_enhanced fsagbase tsc_adjust bmi1 hle avx2
smep bmi2 ermal invpcid cm qmx rdt_a avx512f avx512dq rdseed adx smap clflushopt
clwb intel_pt avx512cd avx512bw avx512vl xsaves xsaveopt xsartic xgetbv1 xsaveq
cq f12_vnni md_clear flush_l1d arch_capabilities

/proc/cpuinfo cache data
cache size: 28160 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)

Tyrone Camarero DS400TG-48R
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Available: 4 nodes (0-3)
node 0 cpus: 0 1 2 5 6 10 11 12 15 16 40 41 42 45 46 50 51 52 55 56
node 0 size: 90116 MB
node 0 free: 94577 MB
node 1 cpus: 3 4 7 8 9 13 14 17 18 19 43 44 47 48 49 53 54 57 58 59
node 1 size: 92387 MB
node 1 free: 96542 MB
node 2 cpus: 20 21 22 25 26 30 31 32 35 36 60 61 62 65 66 70 71 72 75 76
node 2 size: 91349 MB
node 2 free: 96452 MB
node 3 cpus: 23 24 27 28 29 33 34 37 38 39 63 64 67 68 69 73 74 77 78 79
node 3 size: 92216 MB
node 3 free: 96521 MB
node distances:
node 0 1 2 3
0: 10 11 21 21
1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10

From /proc/meminfo
MemTotal: 394852092 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
/sbin/tuned-adm active
Current active profile: throughput-performance
/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release*/etc/*version*
centos-release: CentOS Linux release 8.3.2011
centos-release-upstream: Derived from Red Hat Enterprise Linux 8.3
os-release:
NAME="CentOS Linux"
VERSION="8"
ID="centos"
ID_LIKE="rhel fedora"
VERSION_ID="8"
PLATFORM_ID="platform:el8"
PRETTY_NAME="CentOS Linux 8"
ANSI_COLOR="0;31"
redhat-release: CentOS Linux release 8.3.2011
system-release: CentOS Linux release 8.3.2011
system-release-cpe: cpe:/o:centos:centos:8

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

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Tyrone Camarero DS400TG-48R
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SPECrate®2017_int_peak = 236

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

Test Date: Jan-2021
Hardware Availability: Aug-2020
Software Availability: Dec-2020

Platform Notes (Continued)

uname -a:
    Linux localhost.localdomain 4.18.0-240.el8.x86_64 #1 SMP Fri Sep 25 19:48:47 UTC 2020
    x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): KVM: Mitigation: Split huge pages
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store
    Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1):
    Mitigation: usercopy/swapgs barriers and __user pointer sanitation
CVE-2017-5715 (Spectre variant 2):
    Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort):
    Mitigation: TSX disabled

run-level 3 Jan 29 16:30

SPEC is set to: /home/cpu2017

From /sys/devices/virtual/dmi/id
    Vendor:         Tyrone Systems
    Product:        Tyrone Camarero DS400TG-48R
    Serial:         0123456789

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is 'intended to allow
hardware to be accurately determined', but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
    4x NO DIMM NO DIMM
    12x Samsung M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2666

BIOS:
    BIOS Vendor: American Megatrends Inc.
    BIOS Version: 3.3
    BIOS Date: 02/21/2020
    BIOS Revision: 5.14

(End of data from sysinfo program)
SPEC CPU®2017 Integer Rate Result

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Platform Notes (Continued)
Sysinfo incorrectly parsed dmidecode output. Configured memory speed is 2933.

Compiler Version Notes

==============================================================================
C | 502.gcc_r(peak)
---
Intel(R) C Compiler for applications running on IA-32, Version 2021.1 NextGen
Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
C | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
| 525.x264_r(base, peak) 557.xz_r(base)
---
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
C | 500.perlbench_r(peak) 557.xz_r(peak)
---
Intel(R) C Compiler for applications running on Intel(R) 64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
C | 502.gcc_r(peak)
---
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==============================================================================
C | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
| 525.x264_r(base, peak) 557.xz_r(base)
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(Continued on next page)
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Compiler Version Notes (Continued)

C  | 500.perlbench_r(peak) 557.xz_r(peak)
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Intel(R) C Compiler for applications running on Intel(R) 64,
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C  | 502.gcc_r(peak)
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C  | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
| 525.x264_r(base, peak) 557.xz_r(base)
-----------------------------------------------
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

C  | 500.perlbench_r(peak) 557.xz_r(peak)
-----------------------------------------------
Intel(R) C Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

C++ | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base, peak)
| 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
-----------------------------------------------
Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Fortran | 548.exchange2_r(base, peak)
-----------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.1.1.217 Build 20200306

(Continued on next page)
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Tested by: Tyrone Systems

Compiler Version Notes (Continued)

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Base Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-xCORE-AVX512 -O3 -ffast-math -flto -mfpmath=sse -funroll-loops
-fuse=ld=gold -qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19 compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-1qkmallocc

C++ benchmarks:
-m64 -qnextgen -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -flto -mfpmath=sse
-funroll-loops -fuse=ld=gold -qopt-mem-layout-trans=4

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

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Base Optimization Flags (Continued)

C++ benchmarks (continued):
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-lqkmalloc

Fortran benchmarks:
-m64 -W1,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
-mbranches-within-32B-boundaries
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-lqkmalloc

Peak Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:

(Continued on next page)
## Peak Optimization Flags (Continued)

500.perlbench_r:  
-\Wl, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2)  
-xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4 -fno-strict-overflow  
-mbranches-within-32B-boundaries  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin  
-lqkmalloc

502.gcc_r:  
-\Wl, -z, muldefs -fprofile-generate(pass 1)  
-\Wl, -z, muldefs -fprofile-use=default.profdata(pass 2)  
-xCORE-AVX512 -flto  
-Ofast(pass 1) -O3 -ffast-math -qnextgen -fuse-ld=gold  
-qopt-mem-layout-trans=4 -L/usr/local/je5.0.1-32/lib  
-ljemalloc

505.mcf_r:  
-basepeak = yes

525.x264_r:  
-m64 -qnextgen -std=c11  
-x86-branches-within-32B-boundaries  
-xCORE-AVX512 -flto -O3 -ffast-math  
-flto -qopt-mem-layout-trans=4 -fno-alias  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin  
-ljemalloc

557.xz_r:  
-\Wl, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin  
-ljemalloc

C++ benchmarks:

520.omnetpp_r:  
-basepeak = yes

523.xalancbmk_r:  
-basepeak = yes

531.deepsjeng_r:  
-basepeak = yes

541.leela_r:  
-basepeak = yes

Fortran benchmarks:

548.exchange2_r:  
-basepeak = yes
**SPEC CPU®2017 Integer Rate Result**

**Tyrone Systems**  
(Test Sponsor: Netweb Pte Ltd)  
Tyrone Camarero DS400TG-48R  
(2.10 GHz, Intel Xeon Gold 5218R)  

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The flags files that were used to format this result can be browsed at

http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revB.html

You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64_revA.xml  
http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revB.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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