## SPEC CPU®2017 Integer Rate Result

### Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6238R, 2.20GHz)

<table>
<thead>
<tr>
<th>Copies</th>
<th>SPECrate®2017_int_base = 327</th>
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<tbody>
<tr>
<td>500.perlbench_r 112</td>
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<tr>
<td>502.gcc_r 112</td>
<td>226</td>
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<tr>
<td>505.mcf_r 112</td>
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<tr>
<td>523.xalancbmk_r 112</td>
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<td>525.x264_r 112</td>
<td>421</td>
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<tr>
<td>531.deepsjeng_r 112</td>
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<td>541.leela_r 112</td>
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<tr>
<td>548.exchange2_r 112</td>
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<tr>
<td>557.xz_r 112</td>
<td>199</td>
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</tbody>
</table>

### Hardware
- **CPU Name:** Intel Xeon Gold 6238R
- **Max MHz:** 4000
- **Nominal:** 2200
- **Enabled:** 56 cores, 2 chips, 2 threads/core
- **Orderable:** 1.2 Chips
- **Cache L1:** 32 KB I+ 32 KB D on chip per core
- **Cache L2:** 1 MB I+D on chip per core
- **Cache L3:** 38.5 MB I+D on chip per chip
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
- **Storage:** 1 x 1.2 TB SAS HDD 10K RPM
- **Other:** None
- **OS:** Red Hat Enterprise Linux release 8.2
- **Compiler:** C/C++: Version 19.1.2.275 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.1.2.275 of Intel Fortran Compiler for Linux
- **Parallel:** No
- **Firmware:** Version 4.0.4j released Aug-2019
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** None
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage

### Software
### Test Sponsor: Cisco Systems
### Tested by: Cisco Systems
### CPU2017 License: 9019
### Test Date: Feb-2021
### Hardware Availability: Feb-2020
### Software Availability: Aug-2020

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Translated from the original text.
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6238R, 2.20GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Results Table

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<table>
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</table>

SPECrate®2017_int_base = 327
SPECrate®2017_int_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = 
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

MALLOCONF = "retain: true"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM memory using Redhat Enterprise Linux 8.0 Transparent Huge Pages enabled by default Prior to runcpu invocation Filesystem page cache synced and cleared with:
 sync; echo 3> /proc/sys/vm/drop_caches

(Continued on next page)
General Notes (Continued)

runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7ed8e6e46a485a0011
running on localhost.localdomain Wed Feb 3 01:24:05 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6238R CPU @ 2.20GHz
  2 "physical id"s (chips)
  112 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 28
siblings : 56
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 112
On-line CPU(s) list: 0-111
Thread(s) per core: 2
Core(s) per socket: 28

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CPU2017 License: 9019
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Hardware Availability: Feb-2020
Software Availability: Aug-2020

Platform Notes (Continued)

Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6238R CPU @ 2.20GHz
Stepping: 7
CPU MHz: 1000.039
CPU max MHz: 4000.0000
CPU min MHz: 1000.0000
BogoMIPS: 4400.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 39424K
NUMA node0 CPU(s): 0-3,7-9,14-17,21-23,56-59,63-70,73-77
NUMA node1 CPU(s): 4-6,10-12,18-20,24-27,60-62,66-69,74-76
NUMA node2 CPU(s): 28-31,35-37,42-45,49-51,58-61,64-65,70-73
NUMA node3 CPU(s): 32-34,38-41,46-48,52-55,58-61,64-65
NUMA node4 CPU(s): 0-3,7-9,14-17,21-23,56-59,63-70,73-77
NUMA node5 CPU(s): 4-6,10-12,18-20,24-27,60-62,66-69,74-76
NUMA node6 CPU(s): 28-31,35-37,42-45,49-51,58-61,64-65,70-73
NUMA node7 CPU(s): 32-34,38-41,46-48,52-55,58-61,64-65

Flags:

From numactl --hardware

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

/proc/cpuinfo cache data

From numactl --hardware

(Continued on next page)
Cisco Systems
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Platform Notes (Continued)

CVE-2017-5715 (Spectre variant 2):        Mitigation: Enhanced IBRS, IBPB: conditional, pointer sanitization
rsb filling
tsx_async_abort:                          Mitigation: Clear CPU buffers; SMT vulnerable

run-level 3 Feb 2 23:48

SPEC is set to: /home/cpu2017
Filesystem            Type  Size  Used Avail Use% Mounted on
/dev/mapper/rhel-home xfs   1.1T   21G  1.1T   2% /home

From /sys/devices/virtual/dmi/id
BIOS:    Cisco Systems, Inc. C240M5.4.0.4j.0.0831191216 08/31/2019
Vendor:  Cisco Systems Inc
Product: UCSC-C240-M5L
Serial:  WZP223909MB

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
  24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933

(End of data from sysinfo program)
BIOS version 4.0.4j is available as part of the Unified Computing System (UCS) Server Firmware package version 4.0(4h)

Compiler Version Notes

==============================================================================
C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base)
| 525.x264_r(base) 557.xz_r(base)
------------------------------------------------------------------------------
Intel(R) C Compiler for applications running on Intel(R) 64, Version
19.1.2.275 Build 20200604
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================

==============================================================================
C++     | 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base)
| 541.leela_r(base)
------------------------------------------------------------------------------
Intel(R) C++ Compiler for applications running on Intel(R) 64, Version
19.1.2.275 Build 20200604
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

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Compiler Version Notes (Continued)

------------------------------------------------------------------------------
Fortran | 548.exchange2_r(base)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.1.2.275 Build 20200623
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc
C++ benchmarks:
icpc
Fortran benchmarks:
ifort

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-m64 -qnextgen -std=c11
-Wl, -plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-xCORE-AVX512 -O3 -ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4

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**Base Optimization Flags (Continued)**

C benchmarks (continued):
- -L/usr/local/IntelCompiler19/compilers_and_libraries_2020.3.275/linux/compiler/lib/intel64_lin
- -lqkmalloc

C++ benchmarks:
- -m64 -qnextgen -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
- -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -flto -mfpmath=sse
- -funroll-loops -qopt-mem-layout-trans=4
- -L/usr/local/IntelCompiler19/compilers_and_libraries_2020.3.275/linux/compiler/lib/intel64_lin
- -lqkmalloc

Fortran benchmarks:
- -m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
- -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-mem-layout-trans=4
- -nostandard-realloc-lhs -align array32byte -auto
- -mbranches-within-32B-boundaries
- -L/usr/local/IntelCompiler19/compilers_and_libraries_2020.3.275/linux/compiler/lib/intel64_lin
- -lqkmalloc

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revN.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revN.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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