Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DS400E1U-224R4
(2.90 GHz, Intel Xeon Gold 6226R)

SPECspeed®2017_fp_base = 114
SPECspeed®2017_fp_peak = 116

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

Test Date: Feb-2021
Hardware Availability: Aug-2020

Hardware
CPU Name: Intel Xeon Gold 6226R
Max MHz: 3900
Nominal: 2900
Enabled: 32 cores, 2 chips, 2 threads/core
Orderable: 1.2 (chip)s
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 22 MB I+D on chip per chip
Other: None
Memory: 384 GB (12 x 32 GB 2Rx4 PC4-2933Y-R)
Storage: 1 x 480 GB SATA SSD
Other: None

Software
OS: CentOS Linux release 8.3.2011
4.18.0-240.el8.x86_64
Compiler: C/C++: Version 19.1.1.217 of Intel C/C++ Compiler for Linux Build 20200306;
Fortran: Version 19.1.1.217 of Intel Fortran Compiler for Linux Build 20200306;
Parallel: Yes
Firmware: Version 3.4 released Oct-2020
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS set to prefer performance at the cost of additional power usage
**SPEC CPU®2017 Floating Point Speed Result**

**Tyrone Systems**
(Trademark of Netweb Pte Ltd)
Tyrone Camarero DS400E1U-224R4
(2.90 GHz, Intel Xeon Gold 6226R)

**CPU2017 License:** 006042
**Test Sponsor:** Netweb Pte Ltd
**Tested by:** Tyrone Systems

**Test Date:** Feb-2021
**Hardware Availability:** Aug-2020
**Software Availability:** Dec-2020

---

### Results Table

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<td>123</td>
<td>138</td>
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<td>118</td>
</tr>
</tbody>
</table>

**SPECspeed®2017_fp_base = 114**
**SPECspeed®2017_fp_peak = 116**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

---

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:
- KMP_AFFINITY = "granularity=fine,compact,1,0"
- LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
- MALLOC_CONF = "retain:true"
- OMP_STACKSIZE = "192M"

### General Notes

Binaries compiled on a system with 2x Intel Cascade Lake CPU + 384GB RAM memory using Centos 8.2 x86_64
Transparent Huge Pages enabled by default
Prior to runcpu invocation

Files system cache sync'd and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation built with the Centos 8.2 x86_64, and the system compiler gcc 8.3.1

(Continued on next page)
SPEC CPU®2017 Floating Point Speed Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DS400E1U-224R4
(2.90 GHz, Intel Xeon Gold 6226R)

SPECspeed®2017_fp_base = 114
SPECspeed®2017_fp_peak = 116

BIOS Settings:
- Power Technology = Custom
- Power Performance Tuning = BIOS Controls EPB
- ENERGY_PERF_BIAS_CFG mode = Extreme Performance
- SNC = Enable
- Stale AtoS = Disable
- IMC Interleaving = 1-way Interleave
- Patrol Scrub = Disable

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6538 of 2020-09-24 e8664e66d2d7080afaa89d4b38e2f1c
running on spec Sun Feb 7 15:33:29 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
- model name: Intel(R) Xeon(R) Gold 6226R CPU @ 2.90GHz
  - 2 "physical id"s (chips)
  - 64 "processors"
- cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  - cpu cores: 16
  - siblings: 32
  - physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
  - physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu:
- Architecture: x86_64
- CPU op-mode(s): 32-bit, 64-bit
- Byte Order: Little Endian
- CPU(s): 64
- On-line CPU(s) list: 0-63
- Thread(s) per core: 2
- Core(s) per socket: 16
- Socket(s): 2
- NUMA node(s): 4
- Vendor ID: GenuineIntel
- CPU family: 6
- Model: 85
- Model name: Intel(R) Xeon(R) Gold 6226R CPU @ 2.90GHz

General Notes (Continued)


Platform Notes
SPEC CPU®2017 Floating Point Speed Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)

Tyrone Camarero DS400E1U-224R4
(2.90 GHz, Intel Xeon Gold 6226R)

SPECspeed®2017_fp_base = 114
SPECspeed®2017_fp_peak = 116

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

Platform Notes (Continued)

Stepping: 7
CPU MHz: 3599.973
CPU max MHz: 3900.0000
CPU min MHz: 1200.0000
BogoMIPS: 5800.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 22528K
NUMA node0 CPU(s): 0-3, 8-11, 32-35, 40-43
NUMA node1 CPU(s): 4-7, 12-15, 36-39, 44-47
NUMA node2 CPU(s): 16-19, 24-27, 48-51, 56-59
NUMA node3 CPU(s): 20-23, 28-31, 52-55, 60-63

Flags:
    fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdelpgb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
apefmperef pni pclmulqdq dtss64 ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcu
pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx fl64c
rdand lahf_lm abm 3dnowprefetch cpuid_fault epb cat13 cdcl3 invpcid_single
intel_ppin ssbd mba ibrs ibpb stibp ibrs_enhanced fsgsbase tsc_adjust bmi1 hle avx2
smep bmi2 2rms invpccid cpq mxp rdt_a avx512f avx512d rdseed adx smap clflushopt
clwb intel_pt avx512cd avx512bw avx512vl xsavesopt xsavexc xgetbv1 xsaves cqm_llc
cqm_occup_llc cqm_mbb_total cqm_mbb_local dtherm ida arat pln pts pku ospke
avx512_vnni md_clear flush_ll1d arch_capabilities

/proc/cpuinfo cache data
    cache size: 22528 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
    physical chip.
    available: 4 nodes (0-3)
      node 0 cpus: 0 1 2 3 8 9 10 11 12 13 14 15 36 37 38 39 40 41 42 43
      node 0 size: 91297 MB
      node 0 free: 82367 MB
      node 1 cpus: 4 5 6 7 12 13 14 15 36 37 38 39 44 45 46 47
      node 1 size: 61836 MB
      node 1 free: 53649 MB
      node 2 cpus: 16 17 18 19 24 25 26 27 48 49 50 51 56 57 58 59
      node 2 size: 92736 MB
      node 2 free: 85386 MB
      node 3 cpus: 20 21 22 23 28 29 30 31 52 53 54 55 60 61 62 63
      node 3 size: 93129 MB
      node 3 free: 80046 MB
      node distances:
        node 0 1 2 3
        0: 10 11 21 21

(Continued on next page)
SPEC CPU®2017 Floating Point Speed Result

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Tyrone Camarero DS400E1U-224R4
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CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

Platform Notes (Continued)

1:  11 10 21 21
2:  21 21 10 11
3:  21 21 11 10

From /proc/meminfo
MemTotal:       361832316 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

/sbin/tuned-adm active
  Current active profile: throughput-performance

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has
  performance

From /etc/*release* /etc/*version*
centos-release: CentOS Linux release 8.3.2011
centos-release-upstream: Derived from Red Hat Enterprise Linux 8.3
os-release:
  NAME="CentOS Linux"
  VERSION="8"
  ID="centos"
  ID_LIKE="rhel fedora"
  VERSION_ID="8"
  PLATFORM_ID="platform:el8"
  PRETTY_NAME="CentOS Linux 8"
  ANSI_COLOR="0;31"
redhat-release: CentOS Linux release 8.3.2011
system-release: CentOS Linux release 8.3.2011
system-release-cpe: cpe:/o:centos:centos:8

uname -a:
  Linux spec 4.18.0-240.el8.x86_64 #1 SMP Fri Sep 25 19:48:47 UTC 2020 x86_64 x86_64
  x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-12207 (iTLB Multihit): KVM: Mitigation: Split huge pages
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store
  Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs
  barriers and __user pointer
  sanitization

(Continued on next page)
**SPEC CPU®2017 Floating Point Speed Result**

---

**Tyrone Systems**
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**Tyrone Camarero DS400E1U-224R4**
(2.90 GHz, Intel Xeon Gold 6226R)

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**SPECspeed®2017_fp_base = 114**

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---

**CPU2017 License:** 006042

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**Tested by:** Tyrone Systems

---

**Platform Notes (Continued)**

CVE-2017-5715 (Spectre variant 2):
Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

CVE-2020-0543 (Special Register Buffer Data Sampling):
Not affected

CVE-2019-11135 (TSX Asynchronous Abort):
Mitigation: TSX disabled

---

**run-level 3 Feb 5 15:36**

**SPEC is set to:** /home/cpu2017

**Filesystem** | **Type** | **Size** | **Used** | **Avail** | **Use%** | **Mounted on**
--- | --- | --- | --- | --- | --- | ---
/dev/mapper/cl-home | xfs | 372G | 158G | 215G | 43% | /home

**From /sys/devices/virtual/dmi/id**

**Vendor:** Tyrone Systems

**Product:** Tyrone Camarero DS400E1

**Serial:** S263875X9527668

---

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

**Memory:**
- 12x NO DIMM NO DIMM
- 1x Samsung M393A4K40CB2-CVF 2 rank 2933, configured at 2934
- 11x Samsung M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

**BIOS:**
- BIOS Vendor: American Megatrends Inc.
- BIOS Version: 3.4
- BIOS Date: 10/30/2020
- BIOS Revision: 5.14

---

(End of data from sysinfo program)

---

**Compiler Version Notes**

```
C      619.lbm_s(base, peak) 638.imagick_s(base, peak)
       644.nab_s(base, peak)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
```

---

**C++, C, Fortran**

607.cactuBSSN_s(base, peak)

---

(Continued on next page)
**SPEC CPU®2017 Floating Point Speed Result**

**Tyrone Systems**  
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Tyrone Camarero DS400E1U-224R4  
(2.90 GHz, Intel Xeon Gold 6226R)

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CPU2017 License: 006042  
Test Sponsor: Netweb Pte Ltd  
Tested by: Tyrone Systems

---

**Compiler Version Notes (Continued)**

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.1.1.217 Build 20200306  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.1.1.217 Build 20200306  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.1.1.217 Build 20200306  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

---

Fortran  
603.bwaves_s(base, peak) 649.fotonik3d_s(base, peak)  
654.roms_s(base, peak)

---

Fortran, C  
621.wrf_s(base, peak) 627.cam4_s(base, peak)  
628.pop2_s(base, peak)

---

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.1.1.217 Build 20200306  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

---

**Base Compiler Invocation**

C benchmarks:  
icc

Fortran benchmarks:  
ifort

Benchmarks using both Fortran and C:  
ifort icc

Benchmarks using Fortran, C, and C++:  
icpc icc ifort
SPEC CPU®2017 Floating Point Speed Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DS400E1U-224R4
(2.90 GHz, Intel Xeon Gold 6226R)

SPECspeed®2017_fp_base = 114
SPECspeed®2017_fp_peak = 116

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

Test Date: Feb-2021
Hardware Availability: Aug-2020
Software Availability: Dec-2020

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
   -assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-m64 -std=c11 -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
 -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
 -mbranches-within-32B-boundaries

Fortran benchmarks:
-m64 -Wl,-z,muldefs -DSPEC_OPENMP -xCORE-AVX512 -ipo -O3
 -no-prec-div -qopt-prefetch -ffinite-math-only
 -qopt-mem-layout-trans=4 -qopenmp -nostandard-realloc-lhs
 -mbranches-within-32B-boundaries -L/usr/local/je5.0.1-64/lib -ljemalloc

Benchmarks using both Fortran and C:
-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
 -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
 -DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs
 -L/usr/local/je5.0.1-64/lib -ljemalloc

Benchmarks using Fortran, C, and C++:
-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
 -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
 -DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs
 -L/usr/local/je5.0.1-64/lib -ljemalloc

Peak Compiler Invocation

C benchmarks:
icc

(Continued on next page)
## Peak Compiler Invocation (Continued)

Fortran benchmarks:

```bash
ifort
```

Benchmarks using both Fortran and C:

```bash
ifort icc
```

Benchmarks using Fortran, C, and C++:

```bash
icpc icc ifort
```

## Peak Portability Flags

Same as Base Portability Flags

## Peak Optimization Flags

**C benchmarks:**

- `619.lbm_s`: `basepeak = yes`
- `638.imagick_s`: `basepeak = yes`
- `644.nab_s`:
  - `-m64`
  - `-std=c11`
  - `-Wl,-z,muldefs`
  - `-xCORE-AVX512`
  - `-ipo`
  - `-no-prec-div`
  - `-qopt-prefetch`
  - `-ffinite-math-only`
  - `-Wl,-z,muldefs`
  - `-ipo`
  - `-O3`
  - `-no-prec-div`
  - `-qopt-prefetch`
  - `-ffinite-math-only`
  - `-Wl,-z,muldefs`
  - `-ipo`
  - `-no-prec-div`
  - `-qopt-prefetch`
  - `-ffinite-math-only`
  - `-Wl,-z,muldefs`
  - `-ipo`
  - `-no-prec-div`
  - `-qopt-prefetch`
  - `-ffinite-math-only`
  - `-Wl,-z,muldefs`
  - `-ipo`
  - `-no-prec-div`
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  - `-ipo`
  - `-no-prec-div`
  - `-qopt-prefetch`
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  - `-ipo`
  - `-no-prec-div`
  - `-qopt-prefetch`
  - `-ffinite-math-only`
  - `-Wl,-z,muldefs`
  - `-ipo`
  - `-no-prec-div`
  - `-qopt-prefetch`
  - `-ffinite-math-only`
  - `-Wl,-z,muldefs`
  - `-ipo`
  - `-no-prec-div`
  - `-qopt-prefetch`
  - `-ffinite-math-only`
  - `-Wl,-z,muldefs`
  - `-ipo`
  - `-no-prec-div`
  - `-qopt-prefetch`
  - `-ffinite-math-only`
  - `-Wl,-z,muldefs`
  - `-ipo`
  - `-no-prec-div`
  - `-qopt-prefetch`
  - `-ffinite-math-only`
  - `-Wl,-z,muldefs`

**Fortran benchmarks:**

- `603.bwaves_s`:
  - `-m64`
  - `-Wl,-z,muldefs`
  - `-prof-gen(pass 1)`
  - `-prof-use(pass 2)`
  - `-DSPEC_SUPPRESS_OPENMP`
  - `-DSPEC_OPENMP`
  - `-ipo`
  - `-xCORE-AVX512`
  - `-no-prec-div`
  - `-qopt-prefetch`
  - `-ffinite-math-only`
  - `-qopt-mem-layout-trans=4`
  - `-gopenmp`
  - `-mbranches-within-32B-boundaries`
  - `-L/usr/local/je5.0.1-64/lib`
  - `-ljemalloc`

**649.fotonik3d_s**: Same as `603.bwaves_s`

- `654.roms_s`: `basepeak = yes`

Benchmarks using both Fortran and C:

(Continued on next page)
SPEC CPU®2017 Floating Point Speed Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)

Tyrone Camarero DS400E1U-224R4
(2.90 GHz, Intel Xeon Gold 6226R)

SPECspeed®2017_fp_base = 114
SPECspeed®2017_fp_peak = 116

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

Test Date: Feb-2021
Hardware Availability: Aug-2020
Software Availability: Dec-2020

Peak Optimization Flags (Continued)

621.wrf_s: -m64 -std=c11 -Wl,-z,muldefs -prof-gen(pass 1)
-prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-L/usr/local/je5.0.1-64/lib -ljemalloc

627.cam4_s: basepeak = yes
628.pop2_s: basepeak = yes

Benchmarks using Fortran, C, and C++:
607.cactuBSSN_s: basepeak = yes

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revB.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revB.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.5 on 2021-02-07 05:03:28-0500.
Originally published on 2021-03-02.