**SPEC CPU®2017 Integer Rate Result**

**Tyrone Systems**
(Test Sponsor: Netweb Pte Ltd)

**Tyrone Camarero DS400TR-212R4**
(2.20 GHz, Intel Xeon Gold 5220R)

---

**CPU2017 License:** 006042  
**Test Sponsor:** Netweb Pte Ltd  
**Tested by:** Tyrone Systems  
**Test Date:** Jan-2021  
**Hardware Availability:** Aug-2020  
**Software Availability:** Dec-2020

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<tr>
<th>Benchmark</th>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
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<tr>
<td>500.perlbench_r</td>
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<td>502.gcc_r</td>
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<tr>
<td>557.xz_r</td>
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<td>595</td>
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</tbody>
</table>

---

**Hardware**

- **CPU Name:** Intel Xeon Gold 5220R  
- **Max MHz:** 4000  
- **Nominal:** 2200  
- **Enabled:** 48 cores, 2 chips, 2 threads/core  
- **Orderable:** 1.2 (chip)s  
- **Cache L1:** 32 KB I + 32 KB D on chip per core  
- **L2:** 1 MB I+D on chip per core  
- **L3:** 35.75 MB I+D on chip per chip  
- **Other:** None  
- **Memory:** 384 GB (12 x 32 GB 2Rx4 PC4-2933Y-R, running at 2666)  
- **Storage:** 1 x 480 GB SATA SSD  
- **Other:** None

---

**Software**

- **OS:** CentOS Linux release 8.3.2011  
  4.18.0-240.el8.x86_64  
- **Compiler:** C/C++: Version 19.1.1.217 of Intel C/C++ Compiler Build 20200306 for Linux; Fortran: Version 19.1.1.217 of Intel Fortran Compiler Build 20200306 for Linux  
- **Parallel:** No  
- **Firmware:** Version 3.4 released Oct-2020  
- **File System:** xfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** 32/64-bit  
- **Other:** jemalloc memory allocator V5.0.1  
- **Power Management:** BIOS set to prefer performance at
SPECCPU®2017 Integer Rate Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DS400TR-212R4
(2.20 GHz, Intel Xeon Gold 5220R)

SPECrate®2017_int_base = 296
SPECrate®2017_int_peak = 308

Results Table

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<td>568</td>
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</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Compiler Notes

The inconsistent Compiler version information under Compiler Version section is due to a discrepancy in Intel Compiler.
The correct version of C/C++ compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux
The correct version of Fortran compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = 
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

MALLOCONF = "retain:true"
**SPEC CPU®2017 Integer Rate Result**

**Tyrone Systems**
(Test Sponsor: Netweb Pte Ltd)

**SPEC CPU®2017 Integer Rate Result**

**Tyrone Camarero DS400TR-212R4**
(2.20 GHz, Intel Xeon Gold 5220R)

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**SPECrate®2017_int_base = 296**

**SPECrate®2017_int_peak = 308**

---

**CPU2017 License:** 006042

**Test Sponsor:** Netweb Pte Ltd

**Tested by:** Tyrone Systems

---

**General Notes**

Binaries compiled on a system with 2x Intel Cascade Lake CPU + 384 GB RAM memory using Centos 8.2 x86_64

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3>/proc/sys/vm/drop_caches
```

runcpu command invoked through numactl i.e.:

```
numactl --interleave=all runcpu <etc>
```

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation built with the Centos 8.2 x86_64, and the system compiler gcc 4.8.5 sources available from jemalloc.net or https://github.com/jemalloc/jemalloc/releases

---

**Platform Notes**

**Power Technology = Custom**

**Power Performance Tuning = BIOS Controls EPB**

**ENERGY_PERF_BIAS_CFG mode = Extreme Performance**

**SNC = Enable**

**Stale AtoS = Disable**

**IMC Interleaving = 1-way Interleave**

**Patrol Scrub = Disable**

Sysinfo program /home/cpu2017/bin/sysinfo

Rev: r6538 of 2020-09-24 e8664e66d2d7080afeaa89d4b38e2f1c

running on spec Fri Jan 29 12:41:08 2021

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see

https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Gold 5220R CPU @ 2.20GHz
  2 "physical id"s (chips)
  96 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 24
siblings : 48
  physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29
  physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DS400TR-212R4
(2.20 GHz, Intel Xeon Gold 5220R)

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Tyrone Systems

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

SPECrate®2017_int_base = 296
SPECrate®2017_int_peak = 308

Platform Notes (Continued)

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 96
On-line CPU(s) list: 0-95
Thread(s) per core: 2
Core(s) per socket: 24
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 5220R CPU @ 2.20GHz
Stepping: 7
CPU MHz: 2900.011
CPU max MHz: 4000.0000
CPU min MHz: 1000.0000
BogoMIPS: 4400.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 36608K
NUMA node0 CPU(s): 0-3, 7-9, 13-15, 19, 20, 48-51, 55-57, 61-63, 67, 68
NUMA node1 CPU(s): 4-6, 10-12, 16-18, 21-23, 52-54, 58-60, 64-66, 69-71
NUMA node2 CPU(s): 24-27, 31-33, 37-39, 43, 44, 72-75, 79-81, 85-87, 91, 92
NUMA node3 CPU(s): 28-30, 34-36, 40-42, 45-47, 76-78, 82-84, 88-90, 95-97
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdelgb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtrr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx avx16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_ppn ssbd mba ibrs ibpb stibp ibrs_enhanced fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid cmx mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsavec xconj vt xsavecl cqm_llc cqm_mbm_total cqm_mbm_local dtherm ida arat pln pts pku ospke avx512_vnni md_clear flush_lld arch_capabilities

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 4 nodes (0-3)

(Continued on next page)
## SPEC CPU®2017 Integer Rate Result

**Tyrone Systems**  
**Test Sponsor:** Netweb Pte Ltd  
**Tyrone Camarero DS400TR-212R4**  
**CPU:** 2.20 GHz, Intel Xeon Gold 5220R

### SPECrate®2017

- **SPECrate®2017_int_base = 296**
- **SPECrate®2017_int_peak = 308**

### CPU2017 License: 006042  
**Test Date:** Jan-2021  
**Test Sponsor:** Netweb Pte Ltd  
**Tested by:** Tyrone Systems

### Hardware Availability: Aug-2020  
**Software Availability:** Dec-2020

---

### Platform Notes (Continued)

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<th>Node</th>
<th>CPUs</th>
<th>Size</th>
<th>Free</th>
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<td>0 1 2 3 7 8 9 13 14 15 19 20 48 49 50 51 55 56 57 61 62 63 67 68</td>
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<td></td>
</tr>
<tr>
<td>1</td>
<td>4 5 6 10 11 12 16 17 18 21 22 23 52 53 54 58 59 60 64 65 66 69 70 71</td>
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</tr>
<tr>
<td>2</td>
<td>24 25 26 27 31 32 33 37 38 39 43 44 72 73 74 75 79 80 81 85 86 87 91 92</td>
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<td>3</td>
<td>28 29 30 34 35 36 40 41 42 45 46 47 76 77 78 82 83 84 88 89 90 93 94 95</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **Node distances:**
  - 0: 10 11 21 21
  - 1: 11 10 21 21
  - 2: 21 21 10 11
  - 3: 21 21 11 10

---

From `/proc/meminfo`

- MemTotal: 394855232 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

**/sbin/tuned-adm active**

- Current active profile: throughput-performance

**/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor**

- has performance

From `/etc/*release* /etc/*version*

- centos-release: CentOS Linux release 8.3.2011
- centos-release-upstream: Derived from Red Hat Enterprise Linux 8.3
- os-release:
  - NAME="CentOS Linux"
  - VERSION="8"
  - ID="centos"
  - ID_LIKE="rhel fedora"
  - VERSION_ID="8"
  - PLATFORM_ID="platform:el8"
  - PRETTY_NAME="CentOS Linux 8"
  - ANSI_COLOR="0;31"
- redhat-release: CentOS Linux release 8.3.2011
- system-release: CentOS Linux release 8.3.2011
- system-release-cpe: cpe:/o:centos:centos:8

```
uname -a:
```

(Continued on next page)
X

SPEC CPU®2017 Integer Rate Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DS400TR-212R4
(2.20 GHz, Intel Xeon Gold 5220R)

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CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems
Test Date: Jan-2021
Hardware Availability: Aug-2020
Software Availability: Dec-2020

Platform Notes (Continued)

Linux spec 4.18.0-240.el8.x86_64 #1 SMP Fri Sep 25 19:48:47 UTC 2020 x86_64 x86_64
x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit):
KVM: Mitigation: Split huge pages
CVE-2018-3620 (L1 Terminal Fault):
Not affected
Microarchitectural Data Sampling:
Not affected
CVE-2017-5754 (Meltdown):
Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2018-3639 (Speculative Store Bypass):
Mitigation: usercopy/swaps barriers and __user pointer sanitization
CVE-2017-5753 (Spectre variant 1):
Mitigation: usercopy/swaps barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2):
Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling):
Not affected
CVE-2019-11135 (TSX Asynchronous Abort):
Mitigation: TSX disabled

run-level 3 Jan 29 11:22
SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/mapper/cl-home xfs 372G 156G 216G 42% /home

From /sys/devices/virtual/dmi/id
Vendor: Tyrone Systems
Product: Tyrone Camarero DS400E1
Serial: S263875X9527668

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
12x NO DIMM NO DIMM
12x Samsung M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2666

BIOS:
BIOS Vendor: American Megatrends Inc.
BIOS Version: 3.4
BIOS Date: 10/30/2020
BIOS Revision: 5.14

(End of data from sysinfo program)
Sysinfo incorrectly parsed dmidecode output. Configured memospec.cpu2017.notes_plat_005: BIOS Settings:
### SPEC CPU®2017 Integer Rate Result

**Tyrone Systems**

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Tyrone Camarero DS400TR-212R4  
(2.20 GHz, Intel Xeon Gold 5220R)

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**CPU2017 License:** 006042  
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### Compiler Version Notes

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<th>502.gcc_r(peak)</th>
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Intel(R) C Compiler for applications running on IA-32, Version 2021.1 NextGen  
Build 20200304  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

<table>
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<tr>
<th>C</th>
<th>500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak) 525.x264_r(base, peak) 557.xz_r(base)</th>
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Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1 NextGen Build 20200304  
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Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.1.1.217 Build 20200306  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

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(Continued on next page)
Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DS400TR-212R4
(2.20 GHz, Intel Xeon Gold 5220R)

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

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Test Date: Jan-2021
Hardware Availability: Aug-2020
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Compiler Version Notes (Continued)

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--------------------------------------------------------------------------
C      | 502.gcc_r(peak)
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--------------------------------------------------------------------------
C      | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
       | 525.x264_r(base, peak) 557.xz_r(base)
--------------------------------------------------------------------------
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

--------------------------------------------------------------------------
C      | 500.perlbench_r(peak) 557.xz_r(peak)
--------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

--------------------------------------------------------------------------
C++     | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base, peak)
       | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
--------------------------------------------------------------------------
Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

--------------------------------------------------------------------------
Fortran | 548.exchange2_r(base, peak)
--------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.1.1.217 Build 20200306
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SPEC CPU®2017 Integer Rate Result

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Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)

Tyrone Camarero DS400TR-212R4
(2.20 GHz, Intel Xeon Gold 5220R)

SPECrate®2017_int_base = 296
SPECrate®2017_int_peak = 308

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Test Date: Jan-2021
Tested by: Tyrone Systems
Hardware Availability: Aug-2020
Software Availability: Dec-2020

Base Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-xCORE-AVX512 -O3 -ffast-math -ftito -mfpmath=sse -funroll-loops
-fuse-ld=gold -qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-lqkmalloc

C++ benchmarks:
-m64 -qnextgen -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -ftito -mfpmath=sse
-funroll-loops -fuse-ld=gold -qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-lqkmalloc

Fortran benchmarks:
-m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-mem-layout-trans=4

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

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CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

---

Base Optimization Flags (Continued)

Fortran benchmarks (continued):
- nostandard-realloc-lhs -align array32byte -auto
- mbranches-within-32B-boundaries
- L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
- lqkmalloc

---

Peak Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

---

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

---

Peak Optimization Flags

C benchmarks:
500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)
-xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-strict-overflow
-mbranches-within-32B-boundaries
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
- lqkmalloc

(Continued on next page)
# SPEC CPU®2017 Integer Rate Result

**Tyrone Systems**  
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Tyrone Camarero DS400TR-212R4  
(2.20 GHz, Intel Xeon Gold 5220R)

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## SPECrate®2017_int_base = 296  
SPECrate®2017_int_peak = 308

### Peak Optimization Flags (Continued)

502.gcc_r: -m32  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/ia32_lin  
-std=gnu89  
-W1, -plugin-opt=-x86-branches-within-32B-boundaries  
-W1, -z,muldefs -fprofile-generate(pass 1)  
-fprofile-use=default.profdata(pass 2) -xCORE-AVX512 -flto  
-Ofast(pass 1) -O3 -ffast-math -qnextgen -fuse-ld=gold  
-qopt-mem-layout-trans=4 -L/usr/local/je5.0.1-32/lib  
-ljemalloc

505.mcf_r: basepeak = yes

525.x264_r: -m64 -qnextgen -std=c11  
-W1, -plugin-opt=-x86-branches-within-32B-boundaries  
-W1, -z,muldefs -xCORE-AVX512 -flto -O3 -ffast-math  
-fuse-ld=gold -qopt-mem-layout-trans=4 -fno-alias  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin  
-lqkmalloc

557.xz_r: -W1, -z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin  
-lqkmalloc

### C++ benchmarks:

520.omnetpp_r: basepeak = yes

523.xalancbmk_r: basepeak = yes

531.deepsjeng_r: basepeak = yes

541.leela_r: basepeak = yes

### Fortran benchmarks:

548.exchange2_r: basepeak = yes

The flags files that were used to format this result can be browsed at  
http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revB.html
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You can also download the XML flags sources by saving the following links:

- [http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revB.xml](http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revB.xml)

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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