## SPEC CPU®2017 Floating Point Rate Result

### Inspur Corporation

**Inspur NF5180M5 (Intel Xeon Silver 4110)**

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### Hardware

- **CPU Name:** Intel Xeon Silver 4110
- **Max MHz:** 3000
- **Nominal:** 2100
- **Enabled:** 16 cores, 2 chips, 2 threads/core
- **Orderable:** 1,2 chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 11 MB I+D on chip per chip
- **Other:** None
- **Memory:** 384 GB (12 x 32 GB 2Rx4 PC4-2933Y-R, running at 2400)
- **Storage:** 1 x 1 TB SATA SSD
- **Other:** None

### Software

- **OS:** Red Hat Enterprise Linux release 8.2 (Ootpa) 4.18.0-193.el8.x86_64
- **Compiler:** C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux
- **Parallel:** No
- **Firmware:** Version 4.1.14 released Dec-2020
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** BIOS and OS set to prefer performance at the cost of additional power usage.

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**SPECRate®2017_fp_base = 97.5**

**SPECRate®2017_fp_peak = 98.3**
Inspur Corporation

Inspur NF5180M5 (Intel Xeon Silver 4110)

CPU2017 License: 3358
Test Sponsor: Inspur Corporation
Tested by: Inspur Corporation

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</table>

SPECrate®2017_fp_base = 97.5
SPECrate®2017_fp_peak = 98.3

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"
SCALING_GOVERNOR set to Performance

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/CPU2017/lib/intel64:/home/CPU2017/je5.0.1-64"
MALLOC_CONF = "retain:true"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM memory using Red Hat Enterprise Linux 8.1
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:

(Continued on next page)
Inspur Corporation

Inspur NF5180M5 (Intel Xeon Silver 4110)

SPECrated®2017_fp_base = 97.5
SPECrated®2017_fp_peak = 98.3

CPU2017 License: 3358
Test Sponsor: Inspur Corporation
Tested by: Inspur Corporation

Test Date: May-2021
Hardware Availability: Mar-2019
Software Availability: Jan-2021

General Notes (Continued)

sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numacll i.e.:
numactl --interleave=all runcpu <etc>

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5,
and the system compiler gcc 4.8.5;
sources available from jemalloc.net or

Platform Notes

BIOS configuration:
ENERGY_PERF_BIAS_CFG mode set to Performance
Hardware Prefetch set to Disable
VT Support set to Disable
C1E Support set to Disable
Sub NUMA Cluster (SNC) set to Enable
Intel Hyper Threading Technology set to Enable

Sysinfo program /home/CPU2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16aaca64d
running on localhost.localdomain Tue May 11 13:17:53 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4110 CPU @ 2.10GHz
  2 "physical id"s (chips)
  32 "processors"
  cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 8
  siblings : 16
  physical 0: cores 0 1 2 3 4 5 6 7
  physical 1: cores 0 1 2 3 4 5 6 7

(Continued on next page)
Inspur Corporation

Inspur NF5180M5 (Intel Xeon Silver 4110)

CPU2017 License: 3358
Test Sponsor: Inspur Corporation
Tested by: Inspur Corporation

Test Date: May-2021
Hardware Availability: Mar-2019
Software Availability: Jan-2021

Platform Notes (Continued)

From lscpu from util-linux 2.32.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 32
On-line CPU(s) list: 0-31
Thread(s) per core: 2
Core(s) per socket: 8
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4110 CPU @ 2.10GHz
Stepping: 4
CPU MHz: 2399.965
CPU max MHz: 3000.0000
CPU min MHz: 800.0000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 11264K
NUMA node0 CPU(s): 0-7,16-23
NUMA node1 CPU(s): 8-15,24-31
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single pti intel_pmlnr ssbd mba ibrs ibpb tpr_shadow vmmella flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdmsk rdt_a avx512if avx512dq rdseed adx smap clflushopt clwb intel_pt avx512sd avx512ld avx512vl xsaveopt xsavec xckedv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local dtherm ida arat pln pts pklu ospke md_clear flush_l1d

/proc/cpuinfo cache data
  cache size: 11264 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3 4 5 6 7 16 17 18 19 20 21 22 23
  node 0 size: 192077 MB
  node 0 free: 180542 MB
SPEC CPU®2017 Floating Point Rate Result

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Platform Notes (Continued)

node 1 cpus: 8 9 10 11 12 13 14 15 24 25 26 27 28 29 30 31
node 1 size: 193531 MB
node 1 free: 185951 MB
node distances:
node  0  1
 0:  10  21
 1:  21  10

From /proc/meminfo
MemTotal:       394864224 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

/sbin/tuned-adm active
  Current active profile: throughput-performance

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release*/etc/*version*
NAME="Red Hat Enterprise Linux"
VERSION="8.2 (Ootpa)"
ID="rhel"
ID_LIKE="fedora"
VERSION_ID="8.2"
PLATFORM_ID="platform:el8"
PRETTY_NAME="Red Hat Enterprise Linux 8.2 (Ootpa)"
ANSI_COLOR="0;31"
redhat-release: Red Hat Enterprise Linux release 8.2 (Ootpa)
system-release: Red Hat Enterprise Linux release 8.2 (Ootpa)
system-release-cpe: cpe:/o:redhat:enterprise_linux:8.2:ga
uname -a:
  Linux localhost.localdomain 4.18.0-193.el8.x86_64 #1 SMP Fri Mar 27 14:35:58 UTC 2020
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit):
  KVM: Vulnerable
  Mitigation: PTE Inversion
CVE-2018-3620 (L1 Terminal Fault):
  Mitigation: Clear CPU buffers; SMT vulnerable
Microarchitectural Data Sampling:
CVE-2017-5754 (Meltdown):
  Mitigation: PTI
CVE-2018-3639 (Speculative Store Bypass):
  Mitigation: Speculative Store Bypass disabled via prctl and seccomp

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Platform Notes (Continued)

CVE-2017-5753 (Spectre variant 1):
Mitigation: usercopy/swapgs barriers and __user pointer sanitization

CVE-2017-5715 (Spectre variant 2):
Mitigation: Full generic retpoline, IBPB: conditional, IBRS_FW, STIBP: conditional, RSB filling

CVE-2020-0543 (Special Register Buffer Data Sampling): No status reported

CVE-2019-11135 (TSX Asynchronous Abort):
Mitigation: Clear CPU buffers; SMT vulnerable

run-level 3 May 11 03:31

SPEC is set to: /home/CPU2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/mapper/rhel-home xfs 838G 32G 807G 4% /home

From /sys/devices/virtual/dmi/id
Vendor: Inspur
Product: NF5180M5
Serial: 219243921

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
12x NO DIMM NO DIMM
12x Samsung M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400

BIOS:
BIOS Vendor: American Megatrends Inc.
BIOS Version: 4.1.14
BIOS Date: 12/10/2020
BIOS Revision: 5.14

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C | 519.lbm_r(base, peak) 538.imagick_r(base, peak) 544.nab_r(base, peak)
==============================================================================

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113

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Inspur Corporation

Inspur NF5180M5 (Intel Xeon Silver 4110)  

SPECrates\textsuperscript{2017 \_fp\_peak} = 98.3  
SPECrates\textsuperscript{2017 \_fp\_base} = 97.5

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Compiler Version Notes (Continued)

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------------------------------------------------------------------------
C++  | 508.namd\_r(base, peak) 510.parest\_r(base, peak)
------------------------------------------------------------------------
Intel(R) oneAPI DPC\+/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------
C++, C  | 511.povray\_r(peak)
------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler Classic for applications running on  
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)  
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C++, C  | 511.povray\_r(base) 526.blender\_r(base, peak)
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**Compiler Version Notes (Continued)**

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
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Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
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Inspur NF5180M5 (Intel Xeon Silver 4110)

SPECraten2017_fp_base = 97.5
SPECraten2017_fp_peak = 98.3

CPU2017 License: 3358
Test Sponsor: Inspur Corporation
Tested by: Inspur Corporation

Test Date: May-2021
Hardware Availability: Mar-2019
Software Availability: Jan-2021

Compiler Version Notes (Continued)

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel (R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
Fortran, C      | 521.wrf_r(peak)
==============================================================================
Intel (R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel (R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================

==============================================================================
Fortran, C      | 521.wrf_r(base) 527.cam4_r(base, peak)
==============================================================================
Intel (R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel (R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icx

Benchmarks using both C and C++:
icpx icx

(Continued on next page)
Inspur Corporation

Inspur NF5180M5 (Intel Xeon Silver 4110)

SPECrate®2017_fp_base = 97.5
SPECrate®2017_fp_peak = 98.3

CPU2017 License: 3358
Test Sponsor: Inspur Corporation
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Test Date: May-2021
Hardware Availability: Mar-2019
Software Availability: Jan-2021

Base Compiler Invocation (Continued)

Benchmarks using Fortran, C, and C++:
icpx icx ifort

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.ibm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

C++ benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Fortran benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

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Inspur Corporation

Inspur NF5180M5 (Intel Xeon Silver 4110)

SPECrater®2017_fp_peak = 98.3
SPECrater®2017_fp_base = 97.5

CPU2017 License: 3358
Test Sponsor: Inspur Corporation
Test Date: May-2021
Hardware Availability: Mar-2019
Tested by: Inspur Corporation
Software Availability: Jan-2021

Base Optimization Flags (Continued)

Benchmarks using both Fortran and C:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both C and C++:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-`L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using Fortran, C, and C++:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

Peak Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
521.wrf_r:ifort icc
527.cam4_r:ifort icc

Benchmarks using both C and C++:
511.povray_r:icpc icc

(Continued on next page)
### Peak Compiler Invocation (Continued)

526.blender_r: icpx icx

Benchmarks using Fortran, C, and C++:
- icpx icx ifort

### Peak Portability Flags

Same as Base Portability Flags

### Peak Optimization Flags

C benchmarks:
- 519.lbm_r: basepeak = yes
- 538.imagick_r: basepeak = yes

C++ benchmarks:
- 508.namd_r: basepeak = yes

Fortran benchmarks:

(Continued on next page)
Inspec Corporation

Inspec NF5180M5 (Intel Xeon Silver 4110)

SPECrate®2017_fp_base = 97.5
SPECrate®2017_fp_peak = 98.3

CPU2017 License: 3358
Test Sponsor: Inspec Corporation
Tested by: Inspec Corporation
Test Date: May-2021
Hardware Availability: Mar-2019
Software Availability: Jan-2021

Peak Optimization Flags (Continued)

549.fotonik3d_r: basepeak = yes

554.roms_r: Same as 503.bwaves_r

Benchmarks using both Fortran and C:

521.wrf_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-nostandard-realloc-lhs -align array32byte -auto
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

527.cam4_r: basepeak = yes

Benchmarks using both C and C++:

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

526.blender_r: basepeak = yes

Benchmarks using Fortran, C, and C++:

507.cactuBSSN_r: basepeak = yes

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Inspur-Platform-Settings-V1.9.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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