## SPEC CPU®2017 Floating Point Rate Result

**Cisco Systems**  
Cisco UCS C240 M6 (Intel Xeon Platinum 8380, 2.30GHz)  

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
<th>455</th>
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</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_peak</td>
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</table>

### CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems  

<table>
<thead>
<tr>
<th>Hardware</th>
<th>Software</th>
</tr>
</thead>
</table>
| CPU Name: Intel Xeon Platinum 8380  
Max MHz: 3400  
Nominal: 2300  
Enabled: 80 cores, 2 chips, 2 threads/core  
Orderable: 1,2 Chips  
Cache L1: 32 KB I + 48 KB D on chip per core  
L2: 1.25 MB I+D on chip per core  
L3: 60 MB I+D on chip per core  
Other: None  
Memory: 2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R)  
Storage: 1 x 240 GB SATA SSD  
Other: None | OS: SUSE Linux Enterprise Server 15 SP2  
5.3.18-22-default  
Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;  
Parallel: No  
Firmware: Version 4.2.1c released Jul-2021  
File System: btrfs  
System State: Run level 3 (multi-user)  
Base Pointers: 64-bit  
Peak Pointers: Not Applicable  
Other: jemalloc memory allocator V5.0.1  
Power Management: BIOS and OS set to prefer performance at the cost of additional power usage |
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### Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Platinum 8380, 2.30GHz)

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<td>Cisco Systems</td>
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<td>Software Availability:</td>
<td>Mar-2021</td>
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### Results Table

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</table>

**SPECrate®2017_fp_base = 455**

**SPECrate®2017_fp_peak = Not Run**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The `numactl` mechanism was used to bind copies to processors. The config file option 'submit' was used to generate `numactl` commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by `runcpu` before the start of the run:

LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"

MALLOCONF = "retain:true"

### General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM
memory using opensUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to `runcpu` invocation
Filesystem page cache synced and cleared with:

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Platinum 8380, 2.30GHz)

General Notes (Continued)

test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.


Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
UPI Link Enablement set to 1
UPI Power Management set to Enabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Enhanced CPU performance set to Auto
Energy Efficient Turbo set to Enabled
Processor C6 Report set to Enabled
Processor C1E set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16aca6c64d
running on install Tue Jul  6 21:46:54 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
        model name : Intel(R) Xeon(R) Platinum 8380 CPU @ 2.30GHz
        2 "physical id"'s (chips)
        160 "processors"
        cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
        cpu cores : 40
        siblings : 80

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Platinum 8380, 2.30GHz)

SPECrate®2017_fp_base = 455
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Jul-2021
Tested by: Cisco Systems
Hardware Availability: Apr-2021
Software Availability: Mar-2021

Platform Notes (Continued)

physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 160
On-line CPU(s) list: 0-159
Thread(s) per core: 2
Core(s) per socket: 40
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Platinum 8380 CPU @ 2.30GHz
Stepping: 6
CPU MHz: 3000.000
CPU max MHz: 3400.0000
CPU min MHz: 800.0000
BogoMIPS: 4600.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 61440K
NUMA node0 CPU(s): 0-19, 80-99
NUMA node1 CPU(s): 20-39, 100-119
NUMA node2 CPU(s): 40-59, 120-139
NUMA node3 CPU(s): 60-79, 140-159
Flags:

(Continued on next page)
**Platform Notes (Continued)**

```
/arch_capabilities

/proc/cpuinfo cache data
 cache size : 61440 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
 available: 4 nodes (0-3)
 node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 80 81 82 83 84 85 86 87
           88 89 90 91 92 93 94 95 96 97 98 99
 node 0 size: 515679 MB
 node 0 free: 514971 MB
 node 1 cpus: 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 100 101 102
           103 104 105 106 107 108 109 110 111 112 113 114 115 116 117 118 119
 node 1 size: 516086 MB
 node 1 free: 515487 MB
 node 2 cpus: 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 120 121 122
           123 124 125 126 127 128 129 130 131 132 133 134 135 136 137 138 139
 node 2 size: 516052 MB
 node 2 free: 515692 MB
 node 3 cpus: 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 140 141 142
           143 144 145 146 147 148 149 150 151 152 153 154 155 156 157 158 159
 node 3 size: 516082 MB
 node 3 free: 515667 MB
 node distances:
   node 0  1  2  3
   0:  10 11  20  20
   1:  11 10  20  20
   2:  20 20  10  11
   3:  20 20  11  10

From /proc/meminfo
 MemTotal:       2113435296 kB
 HugePages_Total:       0
 Hugepagesize:       2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
 os-release:
 NAME="SLES"
 VERSION="15-SP2"
 VERSION_ID="15.2"
 PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
 ID="sles"
 ID_LIKE="suse"
```

(Continued on next page)
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CPU2017 License: 9019
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Test Date: Jul-2021

Tested by: Cisco Systems
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Software Availability: Mar-2021

SPECrater®2017_fp_base = 455
SPECrater®2017_fp_peak = Not Run

Platform Notes (Continued)

```
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
    Linux install 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
    x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit):
    Not affected
CVE-2018-3620 (L1 Terminal Fault):
    Not affected
Microarchitectural Data Sampling:
    Not affected
CVE-2017-5754 (Meltdown):
    Not affected
CVE-2018-3639 (Speculative Store Bypass):
    Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1):
    Mitigation: usercopy/swapgs barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2):
    Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling):
    Not affected
CVE-2019-11135 (TSX Asynchronous Abort):
    Not affected

run-level 3 Jul 6 21:34

SPEC is set to: /home/cpu2017
    Filesystem  Type  Size  Used  Avail  Use%  Mounted on
    /dev/sda2   btrfs  222G   15G  206G   7%  /home

From /sys/devices/virtual/dmi/id
    Vendor: Cisco Systems Inc
    Product: UCSC-C240-M6SX
    Serial: WZP24440K0A

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
    Memory:
        32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200

BIOS:
    BIOS Vendor: Cisco Systems, Inc.
    BIOS Version: C240M6.4.2.1c.1.0701210708
    BIOS Date: 07/01/2021
    BIOS Revision: 5.22
```
(Continued on next page)
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Software Availability: Mar-2021

Platform Notes (Continued)

(End of data from sysinfo program)

Compiler Version Notes

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<tr>
<th>C</th>
<th>519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)</th>
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<td>Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,</td>
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<td>Version 2021.1 Build 20201113</td>
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<tr>
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Compiler Version Notes (Continued)

Fortran         | 503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)
-----------------|----------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
                                     Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Fortran, C      | 521.wrf_r(base) 527.cam4_r(base)
-----------------|------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
                                      Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
                                      Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icx
C++ benchmarks:
icpx
Fortran benchmarks:
ifort
Benchmarks using both Fortran and C:
ifort icx
Benchmarks using both C and C++:
icpx icx
Benchmarks using Fortran, C, and C++:
icpx icx ifort

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactusBSSN_r: -DSPEC_LP64

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Base Portability Flags (Continued)

508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-w -std=c11 -m64 -Wl,-z,-muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

C++ benchmarks:
-w -m64 -Wl,-z,-muldefs -xCORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Fortran benchmarks:
-w -m64 -Wl,-z,-muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both Fortran and C:
-w -m64 -std=c11 -Wl,-z,-muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both C and C++:
-w -m64 -std=c11 -Wl,-z,-muldefs -xCORE-AVX512 -Ofast -ffast-math
Cisco Systems

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**Base Optimization Flags (Continued)**

Benchmarks using both C and C++ (continued):
```
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib
```

Benchmarks using Fortran, C, and C++:
```
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib
```

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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