# SPEC CPU®2017 Integer Rate Result

## Cisco Systems

Cisco UCS B200 M6 (Intel Xeon Platinum 8368, 2.40GHz)

<table>
<thead>
<tr>
<th>Software</th>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS</td>
<td>SUSE Linux Enterprise Server 15 SP2</td>
<td></td>
</tr>
<tr>
<td>Compiler</td>
<td>C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux; C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux</td>
<td></td>
</tr>
<tr>
<td>Parallel</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>Firmware</td>
<td>Version 4.2.1 released Jun-2021</td>
<td></td>
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<tr>
<td>File System</td>
<td>btrfs</td>
<td></td>
</tr>
<tr>
<td>System State</td>
<td>Run level 3 (multi-user)</td>
<td></td>
</tr>
<tr>
<td>Base Pointers</td>
<td>64-bit</td>
<td></td>
</tr>
<tr>
<td>Peak Pointers</td>
<td>32/64-bit</td>
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<tr>
<td>Other</td>
<td>jemalloc memory allocator V5.0.1</td>
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</tr>
<tr>
<td>Power Management</td>
<td>BIOS and OS set to prefer performance at the cost of additional power usage</td>
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## Hardware

<table>
<thead>
<tr>
<th>CPU Name</th>
<th>Intel Xeon Platinum 8368</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max MHz</td>
<td>3400</td>
</tr>
<tr>
<td>Nominal</td>
<td>2400</td>
</tr>
<tr>
<td>Enabled</td>
<td>76 cores, 2 chips, 2 threads/core</td>
</tr>
<tr>
<td>Orderable</td>
<td>1.2 Chips</td>
</tr>
<tr>
<td>Cache L1</td>
<td>32 KB I + 48 KB D on chip per core</td>
</tr>
<tr>
<td>L2</td>
<td>1.25 MB I+D on chip per core</td>
</tr>
<tr>
<td>L3</td>
<td>57 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Other</td>
<td>None</td>
</tr>
<tr>
<td>Memory</td>
<td>2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R)</td>
</tr>
<tr>
<td>Storage</td>
<td>1 x 960 GB SATA SSD</td>
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<tr>
<td>Other</td>
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<th>505.mcf_r</th>
<th>520.omnetpp_r</th>
<th>523.xalancbmk_r</th>
<th>525.x264_r</th>
<th>531.deepsjeng_r</th>
<th>541.leela_r</th>
<th>548.exchange2_r</th>
<th>557.xz_r</th>
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<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
</tr>
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<tbody>
<tr>
<td>(527)</td>
<td>(548)</td>
</tr>
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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Jul-2021  
**Hardware Availability:** Jun-2021  
**Software Availability:** Mar-2021  

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## Results Table

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<td>292</td>
<td>564</td>
<td>291</td>
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</tbody>
</table>

**Submit Notes**

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

**Environment Variables Notes**

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH = 
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"
```

```
MALLOC_CONF = "retain:true"
```

**General Notes**

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM memory using openSUSE Leap 15.2

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3>/proc/sys/vm/drop_caches
```

runcpu command invoked through numactl i.e.:
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Platinum 8368, 2.40GHz)

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2021 Standard Performance Evaluation Corporation

SPECrate®2017_int_base = 527
SPECrate®2017_int_peak = 548

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2021
Hardware Availability: Jun-2021
Software Availability: Mar-2021

General Notes (Continued)

numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
UPI Link Enablement set to 1
UPI Power Management set to Enabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Energy Efficient Turbo set to Enabled
Processor C6 Report set to Enabled
Processor C1E set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d running on install Fri Jul 9 22:06:13 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Platinum 8368 CPU @ 2.40GHz
 2 "physical id"s (chips)
 152 "processors"
core, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 38
siblings : 76
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Platinum 8368, 2.40GHz)

SPECrate®2017_int_base = 527
SPECrate®2017_int_peak = 548

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Jul-2021
Tested by: Cisco Systems
Hardware Availability: Jun-2021
Software Availability: Mar-2021

Platform Notes (Continued)

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 152
On-line CPU(s) list: 0-151
Thread(s) per core: 2
Core(s) per socket: 38
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Platinum 8368 CPU @ 2.40GHz
Stepping: 6
CPU MHz: 800.119
CPU max MHz: 3400.0000
CPU min MHz: 800.0000
BogoMIPS: 4800.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 58368K
NUMA node0 CPU(s): 0-37,76-113
NUMA node1 CPU(s): 38-75,114-151
Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pclid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid ept_ad fsqm fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erm sinvpcid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni avx512bw avx512vl xsaveopt xsaveprec xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local wbinvd dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_fractional_tsc dts ept vpid apic sm m等候 capability

/proc/cpuinfo cache data
   cache size : 58368 KB

(Continued on next page)
### Cisco Systems

**Cisco UCS B200 M6 (Intel Xeon Platinum 8368, 2.40GHz)**

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>527</th>
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<tbody>
<tr>
<td>SPECrate®2017_int_peak</td>
<td>548</td>
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</table>

<table>
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<th>CPU2017 License:</th>
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<tr>
<td>Test Sponsor:</td>
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<td>Tested by:</td>
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<tr>
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<td>Hardware Availability:</td>
<td>Jun-2021</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Mar-2021</td>
</tr>
</tbody>
</table>

#### Platform Notes (Continued)

From numactl --hardware

WARNING: a numactl 'node' might or might not correspond to a physical chip.

available: 2 nodes (0-1)

node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100 101 102 103 104 105 106 107 108 109 110 111 112 113
node 0 size: 1031768 MB
node 0 free: 1031065 MB

node 1 cpus: 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100 101 102 103 104 105 106 107 108 109 110 111 112 113
node 1 size: 1032136 MB
node 1 free: 1031354 MB

node distances:

node 0 size: 1031768 MB
node 0 free: 1031065 MB

node distances:

node 0 size: 1032136 MB
node 0 free: 1031354 MB

node distances:

node 0 size: 1031768 MB
node 0 free: 1031065 MB

node distances:

node 0 size: 1032136 MB
node 0 free: 1031354 MB

From /proc/meminfo

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<th>MemTotal:</th>
<th>2113438496 kB</th>
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<tbody>
<tr>
<td>HugePages_Total:</td>
<td>0</td>
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<tr>
<td>Hugepagesize:</td>
<td>2048 kB</td>
</tr>
</tbody>
</table>

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release*/ /etc/*version*

os=release

NAME="SLES"
VERSION="15-SP2"
VERSION_ID="15.2"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:

Linux install 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected

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Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Platinum 8368, 2.40GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Specrate®2017_int_base = 527
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Test Date: Jul-2021
Hardware Availability: Jun-2021
Software Availability: Mar-2021

Platform Notes (Continued)

CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass):
Mitigation: Speculative Store Bypass disabled via prctl and seccomp

CVE-2017-5753 (Spectre variant 1):
Mitigation: usercopy/swapgs barriers and __user pointer sanitization

CVE-2017-5715 (Spectre variant 2):
Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Jul 9 22:02
SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 btrfs 892G 15G 876G 2% /home

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSB-B200-M6
Serial: FCH24097578

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200

BIOS:
BIOS Vendor: Cisco Systems, Inc.
BIOS Version: B200M6.4.2.1.41.0625210158
BIOS Date: 06/25/2021
BIOS Revision: 5.22

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
| C         | 500.perlbench_r(peak) 557.xz_r(peak) |
==============================================================================

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

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Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Platinum 8368, 2.40GHz)

**SPEC CPU®2017 Integer Rate Result**

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<td>Hardware Availability: Jun-2021</td>
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**SPECrate®2017_int_base = 527**

**SPECrate®2017_int_peak = 548**

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**Compiler Version Notes (Continued)**

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<th>C</th>
<th>502.gcc_r(peak)</th>
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Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

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<td>525.x264_r(base, peak) 557.xz_r(base)</td>
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Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

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<thead>
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<th>C</th>
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Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
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<th>C</th>
<th>502.gcc_r(peak)</th>
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Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version 2021.1 Build 20201113
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<th>C</th>
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<td></td>
<td>525.x264_r(base, peak) 557.xz_r(base)</td>
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Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
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(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Platinum 8368, 2.40GHz)

SPECRate®2017_int_base = 527
SPECRate®2017_int_peak = 548

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2021
Hardware Availability: Jun-2021
Software Availability: Mar-2021

Compiler Version Notes (Continued)

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Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
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Base Compiler Invocation

C benchmarks:
  icx

C++ benchmarks:
  icpx

(Continued on next page)
SPECCPU®2017 Integer Rate Result

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SPECrater®2017_int_peak = 548

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Base Compiler Invocation (Continued)

Fortran benchmarks:
ifort

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-lassen /opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

C++ benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-lassen /opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

Fortran benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-auto -mbranches-within-32B-boundaries
-lassen /opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Platinum 8368, 2.40GHz)

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2021
Hardware Availability: Jun-2021
Software Availability: Mar-2021

Peak Compiler Invocation

C benchmarks (except as noted below):
icx

500.perlbench_r: icc
557.xz_r: icc

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:

500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)
-xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-strict-overflow
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

502.gcc_r: -m32
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/ia32_lin
-std=gnu89 -Wl,-z,muldefs -fprofile-generate(pass 1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX512 -flto
-Ofast(pass 1) -O3 -ffast-math -qopt-mem-layout-trans=4

(Continued on next page)
## SPEC CPU®2017 Integer Rate Result

**Cisco Systems**

Cisco UCS B200 M6 (Intel Xeon Platinum 8368, 2.40GHz)

<table>
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<tr>
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<tr>
<td>527</td>
<td>548</td>
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</tbody>
</table>

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### Peak Optimization Flags (Continued)

502.gcc_r (continued):
- mbranches-within-32B-boundaries
- -L/usr/local/jemalloc32-5.0.1/lib -ljemalloc

505.mcf_r: basepeak = yes

525.x264_r: -w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flto
- -O3 -ffast-math -qopt-mem-layout-trans=4 -fno-alias
- mbranches-within-32B-boundaries
- -L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
  -lqkmalloc

557.xz_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- -qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
- -L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
  -lqkmalloc

C++ benchmarks:

520.omnetpp_r: basepeak = yes

523.xalancbmk_r: basepeak = yes

531.deepsjeng_r: basepeak = yes

541.leela_r: basepeak = yes

Fortran benchmarks:

548.exchange2_r: basepeak = yes

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The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:


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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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