## SPEC CPU®2017 Floating Point Rate Result

### Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Silver 4316, 2.30GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
<th>288</th>
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</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_peak</td>
<td>Not Run</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Hardware</th>
<th>Software</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name: Intel Xeon Silver 4316</td>
<td>OS: SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default</td>
</tr>
<tr>
<td>Max MHz: 3400</td>
<td>Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;</td>
</tr>
<tr>
<td>Nominal: 2300</td>
<td>Parallel: No</td>
</tr>
<tr>
<td>Enabled: 40 cores, 2 chips, 2 threads/core</td>
<td>Firmware: Version 4.2.1c released Jul-2021</td>
</tr>
<tr>
<td>Orderable: 1,2 Chips</td>
<td>File System: btrfs</td>
</tr>
<tr>
<td>Cache L1: 32 KB I + 48 KB D on chip per core</td>
<td>System State: Run level 3 (multi-user)</td>
</tr>
<tr>
<td>L2: 1.25 MB I+D on chip per core</td>
<td>Base Pointers: 64-bit</td>
</tr>
<tr>
<td>L3: 30 MB I+D on chip per chip</td>
<td>Peak Pointers: Not Applicable</td>
</tr>
<tr>
<td>Other: None</td>
<td>Other: jemalloc memory allocator V5.0.1</td>
</tr>
<tr>
<td>Memory: 2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R, running at 2666)</td>
<td>Power Management: BIOS and OS set to prefer performance at the cost of additional power usage</td>
</tr>
<tr>
<td>Storage: 1 x 240 GB SATA SSD</td>
<td></td>
</tr>
</tbody>
</table>

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<table>
<thead>
<tr>
<th>Copies</th>
<th>SPECrate®2017_fp_base (288)</th>
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<tr>
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</tr>
<tr>
<td>507.cactuBSSN_r 80</td>
<td></td>
</tr>
<tr>
<td>508.namd_r 80</td>
<td>393</td>
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<tr>
<td>510.parest_r 80</td>
<td>210</td>
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<tr>
<td>511.povray_r 80</td>
<td>160</td>
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<tr>
<td>519.lbm_r 80</td>
<td>317</td>
</tr>
<tr>
<td>521.wrf_r 80</td>
<td>184</td>
</tr>
<tr>
<td>526.blender_r 80</td>
<td>274</td>
</tr>
<tr>
<td>527.cam4_r 80</td>
<td>291</td>
</tr>
<tr>
<td>538.imagick_r 80</td>
<td>297</td>
</tr>
<tr>
<td>544.nab_r 80</td>
<td>80</td>
</tr>
<tr>
<td>549.fotonik3d_r 80</td>
<td>482</td>
</tr>
<tr>
<td>554.roms_r 80</td>
<td>727</td>
</tr>
</tbody>
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Jul-2021
Hardware Availability: Jun-2021
Software Availability: Mar-2021
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Silver 4316, 2.30GHz)

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SPECrate®2017_fp_base = 288
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Results Table

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<th>Ratio</th>
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<tbody>
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<tr>
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<td>394</td>
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<tr>
<td>508.namd_r</td>
<td>80</td>
<td>363</td>
<td>210</td>
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<td>210</td>
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<td>210</td>
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<tr>
<td>510.parest_r</td>
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<td>511.povray_r</td>
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<td>290</td>
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<td>466</td>
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<tr>
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<td>1009</td>
<td>126</td>
<td>1006</td>
<td>126</td>
<td>1003</td>
<td>127</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC_CONF = "retain:true"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM
memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:

(Continued on next page)
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**Tested by:** Cisco Systems  
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### General Notes (Continued)

sync; echo 3> /proc/sys/vm/drop_caches  
runcpu command invoked through numactl i.e.:  
numactl --interleave=all runcpu <etc>

**NA:** The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

**Yes:** The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

**Yes:** The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.


### Platform Notes

**BIOS Settings:**
- Adjacent Cache Line Prefetcher set to Disabled
- DCU Streamer Prefetch set to Disabled
- UPI Link Enablement set to 1
- UPI Power Management set to Enabled
- Sub NUMA Clustering set to Enabled
- LLC Dead Line set to Disabled
- Memory Refresh Rate set to 1x Refresh
- ADDDC Sparing set to Disabled
- Patrol Scrub set to Disabled
- Enhanced CPU performance set to Auto
- Energy Efficient Turbo set to Enabled
- Processor C6 Report set to Enabled
- Processor C1E set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r6538 of 2020-09-24 e8664e66d2d7080afeaa89d4b38e2f1c  
running on localhost Thu Jul 15 10:01:23 2021

**SUT (System Under Test) info as seen by some common utilities.**
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
- model name : Intel(R) Xeon(R) Silver 4316 CPU @ 2.30GHz  
  - 2 "physical id"s (chips)  
  - 80 "processors"
- cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)  
  - cpu cores : 20  
  - siblings : 40

(Continued on next page)
Platform Notes (Continued)

physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 80
On-line CPU(s) list: 0-79
Thread(s) per core: 2
Core(s) per socket: 20
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Silver 4316 CPU @ 2.30GHz
Stepping: 6
CPU MHz: 800.000
CPU max MHz: 3400.0000
CPU min MHz: 800.0000
BogoMIPS: 4600.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 30720K
NUMA node0 CPU(s): 0-9,40-49
NUMA node1 CPU(s): 10-19,50-59
NUMA node2 CPU(s): 20-29,60-69
NUMA node3 CPU(s): 30-39,70-79
Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault ebx cat_13 invpcid_single ssbd mba ibrs ibrd ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni avx512bw avx512vl xsaveopt xsaveprec xsaves xsavec xcksum xsaveopt m gets xsaveopt cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local wbnoiw dtherm ida arat pln pts hwp_act_window hwp_epp hwp_pkg_req avx512vmbi umip pku ospke avx512_vmbi2 gfnl vaes vpcmldqdq avx512_vnni avx512_bitalg tme avx512_vpopcntdq 1a57 rdpid md_clear pconfig flush_l1d arch_capabilities

(Continued on next page)
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Platform Notes (Continued)

/proc/cpuinfo cache data
  cache size: 30720 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 4 nodes (0-3)
    node 0 cpus: 0 1 2 3 4 5 6 7 8 9 40 41 42 43 44 45 46 47 48 49
    node 0 size: 515650 MB
    node 0 free: 514427 MB
    node 1 cpus: 10 11 12 13 14 15 16 17 18 19 50 51 52 53 54 55 56 57 58 59
    node 1 size: 516090 MB
    node 1 free: 515360 MB
    node 2 cpus: 20 21 22 23 24 25 26 27 28 29 60 61 62 63 64 65 66 67 68 69
    node 2 size: 516090 MB
    node 2 free: 515360 MB
    node 3 cpus: 30 31 32 33 34 35 36 37 38 39 70 71 72 73 74 75 76 77 78 79
    node 3 size: 516087 MB
    node 3 free: 515364 MB
    node distances:
      node 0 1 2 3
      0: 10 11 20 20
      1: 11 10 20 20
      2: 20 20 10 11
      3: 20 20 11 10

From /proc/meminfo
  MemTotal: 2113453060kB
  HugePages_Total: 0
  Hugepagesize: 2048kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
    os-release:
      NAME="SLES"
      VERSION="15-SP2"
      VERSION_ID="15.2"
      PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
      ID="sles"
      ID_LIKE="suse"
      ANSI_COLOR="0;32"
      CPE_NAME="cpe:/o:suse:sles:15:sp2"

    uname -a:
    Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
    x86_64 x86_64 GNU/Linux

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Platform Notes (Continued)

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Mitigation: Speculative Store
CVE-2018-3639 (Speculative Store Bypass): Bypass disabled via prctl and
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swaps
cbarriers and __user pointer
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB:
sanitization
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Jul 15 02:26

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 btrfs 222G 14G 207G 7% /home

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSC-C240-M6S
Serial: WZP24460JDQ

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200, configured at 2666

BIOS:
BIOS Vendor: Cisco Systems, Inc.
BIOS Version: C240M6.4.2.1c.1.0701210708
BIOS Date: 07/01/2021
BIOS Revision: 5.22

(End of data from sysinfo program)
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### Compiler Version Notes

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<th>Compiler Version Notes</th>
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</table>
| C         | Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved. |
| C++       | Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved. |
| C++, C    | Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved. |
| C++, Fortran | Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved. |
| Fortran   | Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000  
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Compiler Version Notes (Continued)

------------------------------------------------------------------------------
Fortran, C      | 521.wrf_r(base) 527.cam4_r(base)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icx

Benchmarks using both C and C++:
icpx icx

Benchmarks using Fortran, C, and C++:
icpx icx ifort

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char

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### Base Portability Flags (Continued)

- 527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
- 538.imagick_r: -DSPEC_LP64
- 544.nab_r: -DSPEC_LP64
- 549.fotonik3d_r: -DSPEC_LP64
- 554.roms_r: -DSPEC_LP64

### Base Optimization Flags

**C benchmarks:**
- `-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math`
- `-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4`
- `-mbranches-within-32B-boundaries -ljemalloc`
- `-L/usr/local/jemalloc64-5.0.1/lib`

**C++ benchmarks:**
- `-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto`
- `-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4`
- `-mbranches-within-32B-boundaries -ljemalloc`
- `-L/usr/local/jemalloc64-5.0.1/lib`

**Fortran benchmarks:**
- `-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4`
- `-nostandard-realloc-lhs -align array32byte -auto -mbranches-within-32B-boundaries -ljemalloc`
- `-L/usr/local/jemalloc64-5.0.1/lib`

**Benchmarks using both Fortran and C:**

**Benchmarks using both C and C++:**
- `-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4`
- `-mbranches-within-32B-boundaries -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib`

**Benchmarks using Fortran, C, and C++:**
- `-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math`

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<tr>
<td>288</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

### Base Optimization Flags (Continued)

Benchmarks using Fortran, C, and C++ (continued):

- `-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3`  
- `-no-prec-div -qopt-prefetch -ffinite-math-only`  
- `-qopt-multiple-gather-scatter-by-shuffles`  
- `-mbranches-within-32B-boundaries -nostandard-realloc-lhs`  
- `-align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib`

The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:


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**For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.**

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