Cisco Systems

Cisco UCS C240 M6 (Intel Xeon Silver 4314, 2.40GHz)

**SPECrate®2017_int_base = 233**
**SPECrate®2017_int_peak = 241**

<table>
<thead>
<tr>
<th>Software</th>
<th>Hardware</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS: SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default</td>
<td>CPU Name: Intel Xeon Silver 4314</td>
</tr>
<tr>
<td>Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux; C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux</td>
<td>Max MHz: 3400</td>
</tr>
<tr>
<td>Firmware: Version 4.2.1c released Jul-2021</td>
<td>Nominal: 2400</td>
</tr>
<tr>
<td>File System: btrfs</td>
<td>Enabled: 32 cores, 2 chips, 2 threads/core</td>
</tr>
<tr>
<td>System State: Run level 3 (multi-user)</td>
<td>Orderable: 1.2 Chips</td>
</tr>
<tr>
<td>Base Pointers: 64-bit</td>
<td>Cache L1: 32 KB I + 48 KB D on chip per core</td>
</tr>
<tr>
<td>Peak Pointers: 32/64-bit</td>
<td>L2: 1.25 MB I+D on chip per core</td>
</tr>
<tr>
<td>Other: jemalloc memory allocator V5.0.1</td>
<td>L3: 24 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Power Management: BIOS and OS set to prefer performance at the cost of additional power usage</td>
<td>Other: None</td>
</tr>
</tbody>
</table>

| Test Sponsor: Cisco Systems | Memory: 2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R, running at 2666) |
| Tested by: Cisco Systems | Storage: 1 x 240 GB SATA SSD |
| Hardware Availability: Jun-2021 | Other: None |
| Software Availability: Mar-2021 | |
| Test Date: Jul-2021 | |
| Hardware Availability: Jun-2021 | |
| Test Date: Jul-2021 | |
| Hardware Availability: Jun-2021 | |

---

**Hardware Specifications**

- **CPU Name:** Intel Xeon Silver 4314
- **Max MHz:** 3400
- **Nominal:** 2400
- **Enabled:** 32 cores, 2 chips, 2 threads/core
- **Orderable:** 1.2 Chips
- **Cache L1:** 32 KB I + 48 KB D on chip per core
- **L2:** 1.25 MB I+D on chip per core
- **L3:** 24 MB I+D on chip per chip
- **Other:** None
- **Memory:** 2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R, running at 2666)
- **Storage:** 1 x 240 GB SATA SSD
- **Other:** None

---

**Software Specifications**

- **OS:** SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default
- **Compiler:** C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux; C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux
- **Firmware:** Version 4.2.1c released Jul-2021
- **File System:** btrfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 32/64-bit
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** BIOS and OS set to prefer performance at the cost of additional power usage
## Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>64</td>
<td>651</td>
<td>156</td>
<td>651</td>
<td>157</td>
<td>651</td>
<td>157</td>
<td>64</td>
<td>554</td>
<td>184</td>
<td>555</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>64</td>
<td>459</td>
<td>197</td>
<td>458</td>
<td>198</td>
<td>457</td>
<td>198</td>
<td>64</td>
<td>403</td>
<td>225</td>
<td>404</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>64</td>
<td>256</td>
<td>404</td>
<td>256</td>
<td>404</td>
<td>256</td>
<td>404</td>
<td>64</td>
<td>256</td>
<td>404</td>
<td>256</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>64</td>
<td>562</td>
<td>149</td>
<td>561</td>
<td>150</td>
<td>565</td>
<td>149</td>
<td>64</td>
<td>562</td>
<td>149</td>
<td>561</td>
</tr>
<tr>
<td>523.xalanbmkr</td>
<td>64</td>
<td>228</td>
<td>296</td>
<td>227</td>
<td>297</td>
<td>229</td>
<td>296</td>
<td>64</td>
<td>228</td>
<td>296</td>
<td>227</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>64</td>
<td>236</td>
<td>476</td>
<td>236</td>
<td>476</td>
<td>235</td>
<td>476</td>
<td>64</td>
<td>224</td>
<td>500</td>
<td>225</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>64</td>
<td>422</td>
<td>174</td>
<td>422</td>
<td>174</td>
<td>422</td>
<td>174</td>
<td>64</td>
<td>422</td>
<td>174</td>
<td>422</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>64</td>
<td>623</td>
<td>170</td>
<td>621</td>
<td>171</td>
<td>621</td>
<td>171</td>
<td>64</td>
<td>623</td>
<td>170</td>
<td>621</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>64</td>
<td>356</td>
<td>471</td>
<td>360</td>
<td>466</td>
<td>356</td>
<td>471</td>
<td>64</td>
<td>356</td>
<td>471</td>
<td>360</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>64</td>
<td>533</td>
<td>130</td>
<td>533</td>
<td>130</td>
<td>532</td>
<td>130</td>
<td>64</td>
<td>540</td>
<td>128</td>
<td>540</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## Environment Variables Notes

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH = 
    "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

MALLOCONF = "retain: true"
```

## General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM
memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Silver 4314, 2.40GHz)

SPECrate®2017_int_base = 233
SPECrate®2017_int_peak = 241

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

General Notes (Continued)

runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.


Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
UPI Link Enablement set to 1
UPI Power Management set to Enabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Enhanced CPU performance set to Auto
Energy Efficient Turbo set to Enabled
Processor C6 Report set to Enabled
Processor C1E set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
running on install Mon Jul 19 07:31:33 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
  model name : Intel(R) Xeon(R) Silver 4314 CPU @ 2.40GHz
    2 "physical id"s (chips)
    64 "processors"

  cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
    cpu cores : 16
    siblings : 32
    physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

(Continued on next page)
**Cisco Systems**  
Cisco UCS C240 M6 (Intel Xeon Silver 4314, 2.40GHz)  

---

**SPEC CPU®2017 Integer Rate Result**  
Copyright 2017-2021 Standard Performance Evaluation Corporation

---

**Cisco Systems**  
Cisco UCS C240 M6 (Intel Xeon Silver 4314, 2.40GHz)

---

**SPECrate®2017_int_base = 233**  
**SPECrate®2017_int_peak = 241**

---

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Hardware Availability:** Jun-2021

---

**Test Date:** Jul-2021  
**Tested by:** Cisco Systems  
**Software Availability:** Mar-2021

---

**Platform Notes (Continued)**

```
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 64
On-line CPU(s) list: 0-63
Thread(s) per core: 2
Core(s) per socket: 16
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Silver 4314 CPU @ 2.40GHz
Stepping: 6
CPU MHz: 1680.819
CPU max MHz: 3400.0000
CPU min MHz: 800.0000
BogoMIPS: 4800.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 24576K
NUMA node0 CPU(s): 0-7,32-39
NUMA node1 CPU(s): 8-15,40-47
NUMA node2 CPU(s): 16-23,48-55
NUMA node3 CPU(s): 24-31,56-63
Flags: fpu vme de pmr mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdxelgb rdtscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtpref pmict pciid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd
mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vmmi flexpriority ept vpid ept_ad
fsxgbased tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f
avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni
avx512bw avx512vl xsaveopt xsavec xattrtsx vmpnvms vmpnvms vmpnvms vmpnvms vmpnvms
 językowe memoby xsaveopt xsavec xattrtsx vmpnvms vmpnvms vmpnvms vmpnvms vmpnvms
avx512_bitalg tme avx512_vpopcntdq 1a57 rdpid md_clear pconfig flush_l1d
arch_capabilities
```

(Continued on next page)

---

Page 4  
Standard Performance Evaluation Corporation (info@spec.org)  
https://www.spec.org/
Platform Notes (Continued)

```
cache size : 24576 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 4 nodes (0-3)
 node 0 cpus:  0  1  2  3  4  5  6  7  32  33  34  35  36  37  38  39
 node 0 size: 515684 MB
 node 0 free: 515352 MB
 node 1 cpus:  8  9 10 11 12 13 14 15 40 41 42 43 44 45 46 47
 node 1 size: 516091 MB
 node 1 free: 515754 MB
 node 2 cpus: 16 17 18 19 20 21 22 23 48 49 50 51 52 53 54 55
 node 2 size: 516091 MB
 node 2 free: 515651 MB
 node 3 cpus: 24 25 26 27 28 29 30 31 56 57 58 59 60 61 62 63
 node 3 size: 516054 MB
 node 3 free: 515812 MB
 node distances:
   node 0  1  2  3
   0: 10 11 20 20
   1: 11 10 20 20
   2: 20 20 10 11
   3: 20 20 11 10

From /proc/meminfo
MemTotal:  2113457128 kB
HugePages_Total:       0
Hugepagesize:       2048 kB
/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15-SP2"
    VERSION_ID="15.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
Linux install 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
 x86_64 x86_64 GNU/Linux

(Continued on next page)
### SPEC CPU®2017 Integer Rate Result

**Cisco Systems**

Cisco UCS C240 M6 (Intel Xeon Silver 4314, 2.40GHz)

---

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

---

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>= 233</td>
<td>= 241</td>
</tr>
</tbody>
</table>

**Platform Notes (Continued)**

Kernel self-reported vulnerability status:

- CVE-2018-12207 (iTLB Multihit): Not affected
- CVE-2018-3620 (L1 Terminal Fault): Not affected
- Microarchitectural Data Sampling: Not affected
- CVE-2017-5754 (Meltdown): Not affected
- CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
- CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs barriers and __user pointer sanitation
- CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
- CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
- CVE-2019-11135 (TSX Asynchronous Abort): Not affected

---

**run-level 3 Jul 19 07:29**

**SPEC is set to:** /home/cpu2017

<table>
<thead>
<tr>
<th>Filesystem</th>
<th>Type</th>
<th>Size</th>
<th>Used</th>
<th>Avail</th>
<th>Use%</th>
<th>Mounted on</th>
</tr>
</thead>
<tbody>
<tr>
<td>/dev/sda2</td>
<td>btrfs</td>
<td>222G</td>
<td>37G</td>
<td>184G</td>
<td>17%</td>
<td>/home</td>
</tr>
</tbody>
</table>

From /sys/devices/virtual/dmi/id

- **Vendor:** Cisco Systems Inc  
- **Product:** UCSC-C240-M6S  
- **Serial:** WZP24460JDZ

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

**Memory:**

32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200, configured at 2666

**BIOS:**

- **Vendor:** Cisco Systems, Inc.  
- **Version:** C240M6.4.2.1c.1.0701210708  
- **Date:** 07/01/2021  
- **Revision:** 5.22

(End of data from sysinfo program)
## SPEC CPU®2017 Integer Rate Result

**Cisco Systems**
Cisco UCS C240 M6 (Intel Xeon Silver 4314, 2.40GHz)

**SPECrate®2017_int_base = 233**
**SPECrate®2017_int_peak = 241**

<table>
<thead>
<tr>
<th>CPU2017 License</th>
<th>Test Date</th>
<th>Test Sponsor</th>
<th>Hardware Availability</th>
<th>Tested by</th>
</tr>
</thead>
<tbody>
<tr>
<td>9019</td>
<td>Jul-2021</td>
<td>Cisco Systems</td>
<td>Jun-2021</td>
<td>Cisco Systems</td>
</tr>
</tbody>
</table>

### Compiler Version Notes

```
C       | 500.perlbench_r(peak) 557.xz_r(peak)

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
```

```
C       | 502.gcc_r(peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
```

```
C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
    | 525.x264_r(base, peak) 557.xz_r(base)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
```

```
C       | 500.perlbench_r(peak) 557.xz_r(peak)

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
```

```
C       | 502.gcc_r(peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
```

```
C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
    | 525.x264_r(base, peak) 557.xz_r(base)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
```

(Continued on next page)
## Compiler Version Notes (Continued)

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

---

| C       | 500.perlbench_r(peak) 557.xz_r(peak) |
|-----------------------------|

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

---

| C       | 502.gcc_r(peak) |
|-----------------------------|

Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

---

| C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak) |
|-----------------------------|

| 525.x264_r(base, peak) 557.xz_r(base) |

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

---

| C++     | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base, peak) |
|-----------------------------|

| 531.deepsjeng_r(base, peak) 541.leela_r(base, peak) |

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

---

| Fortran | 548.exchange2_r(base, peak) |
|-----------------------------|

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
## Base Compiler Invocation

C benchmarks:
- icx

C++ benchmarks:
- icpx

Fortran benchmarks:
- ifort

## Base Portability Flags

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Flags</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>-DSPEC_LP64 -DSPEC_LINUX_X64</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>505.mcf_r</td>
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</tr>
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</tr>
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<td>-DSPEC_LP64 -DSPEC_LINUX</td>
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<tr>
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</tr>
<tr>
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</tr>
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<td>541.leela_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>-DSPEC_LP64</td>
</tr>
</tbody>
</table>

## Base Optimization Flags

C benchmarks:
- `-w -std=c11 -m64 -Wl,-z,muldefs -mCORE-AVX512 -O3 -ffast-math`
- `-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4`
- `-mbranches-within-32B-boundaries`
- `-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin`
- `-lgkmalloc`

C++ benchmarks:
- `-w -m64 -Wl,-z,muldefs -mCORE-AVX512 -O3 -ffast-math -flto`
- `-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4`
- `-mbranches-within-32B-boundaries`
- `-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin`
- `-lgkmalloc`

Fortran benchmarks:
- `-w -m64 -Wl,-z,muldefs -mCORE-AVX512 -O3 -ipo -no-prec-div`
- `-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte`
- `-auto -mbranches-within-32B-boundaries`

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Silver 4314, 2.40GHz)

SPECrater®2017_int_base = 233
SPECrater®2017_int_peak = 241

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2021
Hardware Availability: Jun-2021
Software Availability: Mar-2021

Base Optimization Flags (Continued)

Fortran benchmarks (continued):
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

Peak Compiler Invocation

C benchmarks (except as noted below):
icx

500.perlbench_r: icc

557.xz_r: icc

C++ benchmarks:
icpx

Peak Portability Flags

c

Peak Optimization Flags

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Silver 4314, 2.40GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>233</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_peak</td>
<td>241</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2021
Hardware Availability: Jun-2021
Software Availability: Mar-2021

Peak Optimization Flags (Continued)

500.perlbench_r (continued):
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

502.gcc_r: -m32
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/ia32_lin
-std=gnu89 -Wl,-z,muldefs -fprofile-generate(pass 1)
-flags=use=default.profdata(pass 2) -xCORE-AVX512 -flto
-Ofast(pass 1) -O3 -ffast-math -gopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc32-5.0.1/lib -ljemalloc

505.mcf_r: basepeak = yes

525.x264_r: -w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flto
-O3 -ffast-math -gopt-mem-layout-trans=4 -fno-alias
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

557.xz_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-gopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

C++ benchmarks:

520.omnetpp_r: basepeak = yes

523.xalancbmk_r: basepeak = yes

531.deepsjeng_r: basepeak = yes

541.leela_r: basepeak = yes

Fortran benchmarks:

548.exchange2_r: basepeak = yes

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-ICX-revF.xml
## SPEC CPU®2017 Integer Rate Result

**Cisco Systems**
Cisco UCS C240 M6 (Intel Xeon Silver 4314, 2.40GHz)  

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.8 on 2021-07-19 07:31:32-0400.  
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