## SPEC CPU®2017 Floating Point Rate Result

### Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Silver 4316, 2.30GHz)

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
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**Copies**

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
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<tr>
<td>503.bwaves_r</td>
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<tr>
<td>507.cactuBSSN_r</td>
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<tr>
<td>508.namd_r</td>
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<tr>
<td>510.parest_r</td>
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<tr>
<td>554.roms_r</td>
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</table>

**SPECrate®2017_fp_base = 282**
**SPECrate®2017_fp_peak = Not Run**

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<td>Jun-2021</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Dec-2020</td>
</tr>
</tbody>
</table>

### Hardware

- **CPU Name:** Intel Xeon Silver 4316
- **Max MHz:** 3400
- **Nominal:** 2300
- **Enabled:** 40 cores, 2 chips, 2 threads/core
- **Orderable:** 1,2 Chips
- **Cache L1:** 32 KB I + 48 KB D on chip per core
- **L2:** 1.25 MB I+D on chip per core
- **L3:** 30 MB I+D on chip per chip
- **Other:** None
- **Memory:** 2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R, running at 2666)
- **Storage:** 1 x 480 GB SATA SSD
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default
- **Compiler:** C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;
- **Parallel:** No
- **Firmware:** Version 4.2.1c released Jul-2021
- **File System:** btrfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** BIOS and OS set to prefer performance at the cost of additional power usage
## Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Base</th>
<th>Ratio</th>
<th>Seconds</th>
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SPECrate®2017_fp_base = 282
SPECrate®2017_fp_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC_CONF = "retain:true"

## General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Silver 4316, 2.30GHz)

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

General Notes (Continued)

sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
- Adjacent Cache Line Prefetcher set to Disabled
- DCU Streamer Prefetch set to Disabled
- UPI Link Enablement set to Auto
- UPI Power Management set to Disabled
- Sub NUMA Clustering set to Enabled
- LLC Dead Line set to Disabled
- Memory Refresh Rate set to 1x Refresh
- ADDDC Sparing set to Disabled
- Patrol Scrub set to Disabled
- Enhanced CPU performance set to Disabled
- Energy Efficient Turbo set to Enabled
- Processor C6 Report set to Enabled
- Processor C1E set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acaf64d
running on install Fri Jul 30 13:21:30 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
- model name: Intel(R) Xeon(R) Silver 4316 CPU @ 2.30GHz
- 2 "physical id"s (chips)
- 80 "processors"
- cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
- cpu cores: 20
- siblings: 40

(Continued on next page)
Cisco Systems
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**SPECRate®2017_fp_base = 282**

**SPECRate®2017_fp_peak = Not Run**

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**Platform Notes (Continued)**

From `lscpu` from `util-linux 2.33.1`:

- Architecture: x86_64
- CPU op-mode(s): 32-bit, 64-bit
- Byte Order: Little Endian
- Address sizes: 46 bits physical, 57 bits virtual
- CPU(s): 80
- On-line CPU(s) list: 0-79
- Thread(s) per core: 2
- Core(s) per socket: 20
- Socket(s): 2
- NUMA node(s): 4
- Vendor ID: GenuineIntel
- CPU family: 6
- Model: 106
- Model name: Intel(R) Xeon(R) Silver 4316 CPU @ 2.30GHz
- Stepping: 6
- CPU MHz: 3372.455
- CPU max MHz: 3400.0000
- CPU min MHz: 800.0000
- BogoMIPS: 4600.00
- Virtualization: VT-x
- L1d cache: 48K
- L1i cache: 32K
- L2 cache: 1280K
- L3 cache: 30720K
- NUMA node0 CPU(s): 0-9, 40-49
- NUMA node1 CPU(s): 10-19, 50-59
- NUMA node2 CPU(s): 20-29, 60-69
- NUMA node3 CPU(s): 30-39, 70-79
- Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
- pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
- lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
- aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
- xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
- avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd
- mba ibrs ibpb stibp ibrs Enhanced tpr_shadow vmni flexpriority ept vpid ept_ad
- fs.gsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f
- avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha_ni
- avx512bw avx512vl xsaveopt xsavec xsaveopt xsavec xsaveopt xsave cqm_llc cqm_occup_llc cqm_mbb_total
- cqm_mbb_local wbinvd dtherm ida arat pln pts hwp hwp_act_window hwp_epp
- hwp_pkg_req avx512vbmi umip pku ospke avx512_vbmi2 gfn vaes vpcmnlqsd avx512_vnni
- avx512_bitalg tme avx512_vpopcntdq la57 rdpid md_clear pconfig flush_l1d
- arch_capabilities

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Platform Notes (Continued)

/proc/cpuinfo cache data
  cache size : 30720 KB

From numactl --hardware
  WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 4 nodes (0-3)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 40 41 42 43 44 45 46 47 48 49
  node 0 size: 515527 MB
  node 0 free: 515141 MB
  node 1 cpus: 10 11 12 13 14 15 16 17 18 19 50 51 52 53 54 55 56 57 58 59
  node 1 size: 516090 MB
  node 1 free: 515743 MB
  node 2 cpus: 20 21 22 23 24 25 26 27 28 29 60 61 62 63 64 65 66 67 68 69
  node 2 size: 516057 MB
  node 2 free: 515743 MB
  node 3 cpus: 30 31 32 33 34 35 36 37 38 39 70 71 72 73 74 75 76 77 78 79
  node 3 size: 516087 MB
  node 3 free: 515807 MB
  node distances:
    node 0  1   2   3
    0:  10  11  20  20
    1:  11  10  20  20
    2:  20  20  10  11
    3:  20  20  11  10

From /proc/meminfo
  MemTotal:       2113292532 kB
  HugePages_Total:       0
  Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15-SP2"
    VERSION_ID="15.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
  Linux install 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
  x86_64 x86_64 GNU/Linux

(Continued on next page)
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Platform Notes (Continued)

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Speculative Store Bypass) mitigation: usercopy/swapgs barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Jul 30 13:20

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda4 btrfs 445G 16G 428G 4% /home

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSB-B200-M6
Serial: FCH24097576

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200, configured at 2666

BIOS:
BIOS Vendor: Cisco Systems, Inc.
BIOS Version: B200M6.4.2.1c.10.0723211453
BIOS Date: 07/23/2021
BIOS Revision: 5.22

(End of data from sysinfo program)
## Compiler Version Notes

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<tr>
<th>C</th>
<th>519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)</th>
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<tbody>
<tr>
<td>Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113</td>
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Compiler Version Notes (Continued)

Fortran, C      | 521.wrf_r(base) 527.cam4_r(base)
------------------------------------------------------------------------------
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Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icx

Benchmarks using both C and C++:
icpx icx

Benchmarks using Fortran, C, and C++:
icpx icx ifort

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char

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**Base Portability Flags (Continued)**

527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

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**Base Optimization Flags**

**C benchmarks:**
- `-w` `-std=c11` `-m64` `-Wl,-z,muldefs` `-xCORE-AVX512` `-Ofast` `-ffast-math`
- `-flto` `-mfpmath=sse` `-funroll-loops` `-qopt-mem-layout-trans=4`
- `-mbranches-within-32B-boundaries` `-ljemalloc`
- `-L/usr/local/jemalloc64-5.0.1/lib`

**C++ benchmarks:**
- `-w` `-m64` `-Wl,-z,muldefs` `-xCORE-AVX512` `-Ofast` `-ffast-math` `-flto`
- `-mfpmath=sse` `-funroll-loops` `-qopt-mem-layout-trans=4`
- `-mbranches-within-32B-boundaries` `-ljemalloc`
- `-L/usr/local/jemalloc64-5.0.1/lib`

**Fortran benchmarks:**
- `-w` `-m64` `-Wl,-z,muldefs` `-xCORE-AVX512` `-O3` `-ipo` `-no-prec-div`
- `-qopt-prefetch` `-ffinite-math-only`
- `-qopt-multiple-gather-scatter-by-shuffles` `-qopt-mem-layout-trans=4`
- `-nostandard-realloc-lhs` `-align array32byte` `-auto`
- `-mbranches-within-32B-boundaries` `-ljemalloc`
- `-L/usr/local/jemalloc64-5.0.1/lib`

**Benchmarks using both Fortran and C:**
- `-w` `-m64` `-std=c11` `-Wl,-z,muldefs` `-xCORE-AVX512` `-Ofast` `-ffast-math`
- `-flto` `-mfpmath=sse` `-funroll-loops` `-qopt-mem-layout-trans=4` `-O3` `-ipo`
- `-no-prec-div` `-qopt-prefetch` `-ffinite-math-only`
- `-qopt-multiple-gather-scatter-by-shuffles` `-qopt-mem-layout-trans=4`
- `-mbranches-within-32B-boundaries` `-ljemalloc`
- `-L/usr/local/jemalloc64-5.0.1/lib`

**Benchmarks using both C and C++:**
- `-w` `-m64` `-std=c11` `-Wl,-z,muldefs` `-xCORE-AVX512` `-Ofast` `-ffast-math`
- `-flto` `-mfpmath=sse` `-funroll-loops` `-qopt-mem-layout-trans=4`
- `-mbranches-within-32B-boundaries` `-ljemalloc`
- `-L/usr/local/jemalloc64-5.0.1/lib`

**Benchmarks using Fortran, C, and C++:**
- `-w` `-m64` `-std=c11` `-Wl,-z,muldefs` `-xCORE-AVX512` `-Ofast` `-ffast-math`

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Silver 4316, 2.30GHz)

SPECratenospe diff = 282
SPECratenospe peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2021
Hardware Availability: Jun-2021
Software Availability: Dec-2020

Base Optimization Flags (Continued)

Benchmarks using Fortran, C, and C++ (continued):
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-ICX-revF.xml

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