Cisco Systems

Cisco UCS B200 M6 (Intel Xeon Gold 6346, 3.10GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Threads

<table>
<thead>
<tr>
<th>Test</th>
<th>Base</th>
<th>Peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>32</td>
<td>7.33</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>32</td>
<td>11.0</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>32</td>
<td>10.8</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>32</td>
<td>13.8</td>
</tr>
<tr>
<td>623.xalancbmk_s</td>
<td>32</td>
<td>17.4</td>
</tr>
<tr>
<td>625.x264_s</td>
<td>32</td>
<td>6.08</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>32</td>
<td>5.03</td>
</tr>
<tr>
<td>641.leela_s</td>
<td>32</td>
<td>20.0</td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>32</td>
<td>21.1</td>
</tr>
<tr>
<td>657.xz_s</td>
<td>32</td>
<td></td>
</tr>
</tbody>
</table>

**SPECspeed®2017_int_base** = 11.9
**SPECspeed®2017_int_peak** = Not Run

**Hardware**

CPU Name: Intel Xeon Gold 6346
Max MHz: 3600
Nominal: 3100
Enabled: 32 cores, 2 chips
Orderable: 1.2 Chips
Cache L1: 32 KB I + 48 KB D on chip per core
L2: 1.25 MB I+D on chip per core
L3: 36 MB I+D on chip per chip
Other: None
Memory: 2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R)
Storage: 1 x 480 GB SATA SSD
Other: None

**Software**

OS: SUSE Linux Enterprise Server 15 SP2
Compiler: C/C++ Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux;
Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;
Parallel: Yes
Firmware: Version 4.2.1c released Jul-2021
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS and OS set to prefer performance at the cost of additional power usage
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Cisco UCS B200 M6 (Intel Xeon Gold 6346, 3.10GHz)  

SPECSpeed®2017_int_base = 11.9  
SPECSpeed®2017_int_peak = Not Run

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Test Date: Jul-2021  
Tested by: Cisco Systems  
Hardware Availability: Jun-2021  
Software Availability: Dec-2020

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Base</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Peak</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>600:perlbench_s</td>
<td>32</td>
<td>242</td>
<td>7.33</td>
<td>243</td>
<td>7.31</td>
<td>241</td>
<td>7.37</td>
<td></td>
<td></td>
</tr>
<tr>
<td>602:gcc_s</td>
<td>32</td>
<td>363</td>
<td>11.0</td>
<td>361</td>
<td>11.0</td>
<td>363</td>
<td>11.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>605:mcf_s</td>
<td>32</td>
<td>237</td>
<td>19.9</td>
<td>240</td>
<td>19.6</td>
<td>237</td>
<td>19.9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>620:omnetpp_s</td>
<td>32</td>
<td>151</td>
<td>10.8</td>
<td>150</td>
<td>10.9</td>
<td>155</td>
<td>10.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>623:xalancbmk_s</td>
<td>32</td>
<td>103</td>
<td>13.7</td>
<td>103</td>
<td>13.8</td>
<td>103</td>
<td>13.8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>625:x264_s</td>
<td>32</td>
<td>101</td>
<td>17.4</td>
<td>102</td>
<td>17.4</td>
<td>101</td>
<td>17.4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>631:deepsjeng_s</td>
<td>32</td>
<td>236</td>
<td>6.08</td>
<td>236</td>
<td>6.06</td>
<td>236</td>
<td>6.08</td>
<td></td>
<td></td>
</tr>
<tr>
<td>641:leela_s</td>
<td>32</td>
<td>339</td>
<td>5.03</td>
<td>339</td>
<td>5.03</td>
<td>339</td>
<td>5.03</td>
<td></td>
<td></td>
</tr>
<tr>
<td>648:exchange2_s</td>
<td>32</td>
<td>147</td>
<td>20.0</td>
<td>147</td>
<td>20.0</td>
<td>147</td>
<td>20.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>657:sz_s</td>
<td>32</td>
<td>268</td>
<td>23.1</td>
<td>268</td>
<td>23.1</td>
<td>268</td>
<td>23.1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC_CONF = "retain:true"
OMP_STACKSIZE = "192M"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
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Cisco UCS B200 M6 (Intel Xeon Gold 6346, 3.10GHz)

| SPECspeed®2017_int_base = 11.9 |
| SPECspeed®2017_int_peak = Not Run |

General Notes (Continued)

numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel Hyper-Threading Technology set to Disabled
DCU Streamer Prefetch set to Disabled
UPI Link Enablement set to Auto
UPI Power Management set to Disabled
Sub NUMA Clustering set to Disabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Enhanced CPU performance set to Auto
Energy Efficient Turbo set to Enabled
Processor C6 Report set to Enabled
Processor C1E set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acaf64d running on install Thu Jul 29 01:32:22 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6346 CPU @ 3.10GHz
  2 "physical id"s (chips)
  32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
siblings : 16
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

(Continued on next page)
## Platform Notes (Continued)

From `lscpu` from `util-linux 2.33.1`:

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Architecture</td>
<td>x86_64</td>
</tr>
<tr>
<td>CPU op-mode(s)</td>
<td>32-bit, 64-bit</td>
</tr>
<tr>
<td>Byte Order</td>
<td>Little Endian</td>
</tr>
<tr>
<td>Address sizes</td>
<td>46 bits physical, 57 bits virtual</td>
</tr>
<tr>
<td>CPU(s)</td>
<td>32</td>
</tr>
<tr>
<td>On-line CPU(s) list</td>
<td>0-31</td>
</tr>
<tr>
<td>Thread(s) per core</td>
<td>1</td>
</tr>
<tr>
<td>Core(s) per socket</td>
<td>16</td>
</tr>
<tr>
<td>Socket(s)</td>
<td>2</td>
</tr>
<tr>
<td>NUMA node(s)</td>
<td>2</td>
</tr>
<tr>
<td>Vendor ID</td>
<td>GenuineIntel</td>
</tr>
<tr>
<td>CPU family</td>
<td>6</td>
</tr>
<tr>
<td>Model</td>
<td>106</td>
</tr>
<tr>
<td>Model name</td>
<td>Intel(R) Xeon(R) Gold 6346 CPU @ 3.10GHz</td>
</tr>
<tr>
<td>Stepping</td>
<td>6</td>
</tr>
<tr>
<td>CPU MHz</td>
<td>1194.373</td>
</tr>
<tr>
<td>CPU max MHz</td>
<td>3600.0000</td>
</tr>
<tr>
<td>CPU min MHz</td>
<td>800.0000</td>
</tr>
<tr>
<td>BogoMIPS</td>
<td>6200.00</td>
</tr>
<tr>
<td>Virtualization</td>
<td>VT-x</td>
</tr>
<tr>
<td>L1d cache</td>
<td>48K</td>
</tr>
<tr>
<td>L1l cache</td>
<td>32K</td>
</tr>
<tr>
<td>L2 cache</td>
<td>1280K</td>
</tr>
<tr>
<td>L3 cache</td>
<td>36864K</td>
</tr>
<tr>
<td>NUMA node0 CPU(s)</td>
<td>0-15</td>
</tr>
<tr>
<td>NUMA node1 CPU(s)</td>
<td>16-31</td>
</tr>
<tr>
<td>Flags:</td>
<td>fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtechnology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtrunc pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3nowprefetch cpuid_fault ebpx cat_13 invpcid_single ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid ept_ad fsqmbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqg rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha_ni avx512bw avx512vl xsaveopt xsavec xsavec xsave xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local wbinvd dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req avx512vmbi umip pku ospke avx512_vbmi2 gfnq vaes vpcmfdqd avx512_vnni avx512里斯al tme avx512_upopcndtq 1a57 rdpid md_clear pconfig flush_l1d arch_capabilities</td>
</tr>
<tr>
<td>/proc/cpuinfo cache data</td>
<td>cache size: 364 KB</td>
</tr>
</tbody>
</table>

From `numactl --hardware`
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6346, 3.10GHz)

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SPECspeed®2017_int_base = 11.9
SPECspeed®2017_int_peak = Not Run

Test Date: Jul-2021
Hardware Availability: Jun-2021
Software Availability: Dec-2020

Platform Notes (Continued)

WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
node 0 size: 1031623 MB
node 0 free: 1031098 MB
node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
node 1 size: 1032150 MB
node 1 free: 1031712 MB
node distances:
node 0 1
0: 10 20
1: 20 10

From /proc/meminfo
MemTotal: 2113305080 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15-SP2"
VERSION_ID="15.2"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
Linux install 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2018-3639 (Speculative Store Bypass): Mitigation: usercopy/swaps barriers and __user pointer
CVE-2017-5753 (Spectre variant 1):

(Continued on next page)
SPEC CPU®2017 Integer Speed Result

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Platform Notes (Continued)

CVE-2017-5715 (Spectre variant 2):
Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
sanitization
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Jul 29 01:19
SPEC is set to: /home/cpu2017

Filesystem  Type   Size  Used Avail Use% Mounted on
/dev/sda4   btrfs 445G 16G 428G  4% /home

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSB-B200-M6
Serial: FCH2409756

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200

BIOS:
BIOS Vendor: Cisco Systems, Inc.
BIOS Version: B200M6.4.2.1c.10.0723211453
BIOS Date: 07/23/2021
BIOS Revision: 5.22

(End of data from sysinfo program)

Compiler Version Notes

C       | 600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base)
| 625.x264_s(base) 657.xz_s(base)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

C++      | 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)
| 641.leela_s(base)

(Continued on next page)
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SPECSpeed®2017_int_base = 11.9
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Compiler Version Notes (Continued)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Fortran | 648.exchange2_s(base)

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64
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---

### Base Optimization Flags

- **C benchmarks:**
  - -DSPEC_OPENMP
  - -std=c11
  - -m64
  - -fiopenmp
  - -Wl,-z,muldefs
  - -xCORE-AVX512
  - -O3
  - -ffast-math
  - -flto
  - -mfpmath=sse
  - -funroll-loops
  - -L/usr/local/jemalloc64-5.0.1/lib
  - -ljemalloc

- **C++ benchmarks:**
  - -DSPEC_OPENMP
  - -m64
  - -Wl,-z,muldefs
  - -xCORE-AVX512
  - -O3
  - -ffast-math
  - -flto
  - -mfpmath=sse
  - -funroll-loops
  - -qopt-mem-layout-trans=4
  - -mbranches-within-32B-boundaries
  - -L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin/
  - -lqkmalloc

- **Fortran benchmarks:**
  - -m64
  - -xCORE-AVX512
  - -O3
  - -ipo
  - -no-prec-div
  - -qopt-mem-layout-trans=4
  - -nostandard-realloc-lhs
  - -align array32byte
  - -auto
  - -mbranches-within-32B-boundaries

---

The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:


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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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