## Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Silver 4314, 2.40GHz)

| SPECspeed\textsuperscript{\textregistered}2017\_fp\_base | 149 |
| SPECspeed\textsuperscript{\textregistered}2017\_fp\_peak | Not Run |

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Aug-2021  
**Hardware Availability:** Apr-2021  
**Software Availability:** Dec-2020

### Hardware

| CPU Name: Intel Xeon Silver 4314  
| Max MHz: 3400  
| Nominal: 2400  
| Enabled: 32 cores, 2 chips  
| Orderable: 1.2 Chips  
| Cache L1: 32 KB I + 48 KB D on chip per core  
| L2: 1.25 MB I+D on chip per core  
| L3: 24 MB I+D on chip per chip  
| Other: None  
| Memory: 2 TB (32 x 64 GB 2Rx4 PC4-3200V-R, running at 2666)  
| Storage: 1 x 480 GB SATA SSD  
| Other: None |

### Software

| OS: SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default  
| Compiler: Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux; C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux  
| Parallel: Yes  
| Firmware: Version 4.2.1c released Jul-2021  
| File System: btrfs  
| System State: Run level 3 (multi-user)  
| Base Pointers: 64-bit  
| Peak Pointers: Not Applicable  
| Other: jemalloc memory allocator V5.0.1  
| Power Management: BIOS and OS set to prefer performance at the cost of additional power usage |

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[Graph](#)
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SPEC CPU®2017 Floating Point Speed Result

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SPEC CPU®2017 Floating Point Speed Result

Cisco Systems

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SPECspeed®2017_fp_base = 149

SPECspeed®2017_fp_peak = Not Run

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>603.bwaves_s</td>
<td>32</td>
<td>104</td>
<td>567</td>
<td>104</td>
<td>567</td>
<td>105</td>
<td>563</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
<td>32</td>
<td>93.4</td>
<td>178</td>
<td>96.3</td>
<td>173</td>
<td>94.0</td>
<td>177</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>619.lbm_s</td>
<td>32</td>
<td>47.6</td>
<td>110</td>
<td>54.4</td>
<td>96.3</td>
<td>47.7</td>
<td>110</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>621.wrf_s</td>
<td>32</td>
<td>94.9</td>
<td>139</td>
<td>95.7</td>
<td>138</td>
<td>94.7</td>
<td>140</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>627.cam4_s</td>
<td>32</td>
<td>95.0</td>
<td>93.3</td>
<td>94.2</td>
<td>94.1</td>
<td>94.5</td>
<td>93.8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>628.pop2_s</td>
<td>32</td>
<td>156</td>
<td>76.1</td>
<td>159</td>
<td>74.9</td>
<td>157</td>
<td>75.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>638.imagick_s</td>
<td>32</td>
<td>103</td>
<td>140</td>
<td>103</td>
<td>140</td>
<td>104</td>
<td>139</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>644.nab_s</td>
<td>32</td>
<td>76.5</td>
<td>228</td>
<td>76.5</td>
<td>228</td>
<td>76.4</td>
<td>229</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>32</td>
<td>99.1</td>
<td>92.0</td>
<td>98.8</td>
<td>92.3</td>
<td>99.3</td>
<td>91.8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>654.roms_s</td>
<td>32</td>
<td>90.4</td>
<td>174</td>
<td>91.2</td>
<td>173</td>
<td>89.9</td>
<td>175</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
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SPECspeed®2017_fp_peak = Not Run

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOCONF = "retain: true"
OMP_STACKSIZE = "192M"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3 > /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:

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Cisco UCS B200 M6 (Intel Xeon Silver 4314, 2.40GHz)

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

General Notes (Continued)

numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel Hyper-Threading Technology set to Disabled
DCU Streamer Prefetch set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Energy Efficient Turbo set to Enabled
Processor C6 Report set to Enabled
Processor C1E set to Enabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acaf64d running on Thu Aug 5 14:28:05 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4314 CPU @ 2.40GHz
2 "physical id"s (chips)
32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
siblings : 16
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian

(Continued on next page)
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Test Date: Aug-2021
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Platform Notes (Continued)

Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 32
On-line CPU(s) list: 0-31
Thread(s) per core: 1
Core(s) per socket: 16
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Silver 4314 CPU @ 2.40GHz
Stepping: 6
CPU MHz: 1340.317
CPU max MHz: 3400.0000
CPU min MHz: 800.0000
BogoMIPS: 4800.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 24576K
NUMA node0 CPU(s): 0-7
NUMA node1 CPU(s): 8-15
NUMA node2 CPU(s): 16-23
NUMA node3 CPU(s): 24-31

Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave f16c rdrand lahf_lm abm 3nowprefetch cpuid_fault epb cat_13 invpcid_single ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid ept_ad fs静静地 sd fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ets invpcid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni avx512bw avx512vl xsaveopt xsavec xsaveopt xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbb_local wbnoinvd dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req avx512vbmi umip pku ospke avx512_vbmi2 gfnf vaes vpclmulqdq avx512_vnni avx512_latalg tm avx512_vpopcntdq la57 rdr did md_clear pconfig flush_l1d arch_capabilities

/oproc/cpuinfo cache data
  cache size : 24576 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 4 nodes (0-3)
  node 0 cpus: 0 1 2 3 4 5 6 7

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Platform Notes (Continued)

node 0 size: 515529 MB
node 0 free: 515091 MB
node 1 cpus: 8 9 10 11 12 13 14 15
node 1 size: 516093 MB
node 1 free: 515774 MB
node 2 cpus: 16 17 18 19 20 21 22 23
node 2 size: 516059 MB
node 2 free: 515442 MB
node 3 cpus: 24 25 26 27 28 29 30 31
node 3 size: 516090 MB
node 3 free: 512564 MB
node distances:
node 0 1 2 3
0: 10 11 20 20
1: 11 10 20 20
2: 20 20 10 11
3: 20 20 11 10

From /proc/meminfo
MemTotal: 2113304320 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release*/etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15-SP2"
    VERSION_ID="15.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
  Linux install 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
  x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Silver 4314, 2.40GHz)  SPECspec®2017_fp_base = 149
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<table>
<thead>
<tr>
<th>Platform Notes (Continued)</th>
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<tbody>
<tr>
<td>CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp</td>
</tr>
<tr>
<td>CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs barriers and __user pointer sanitization</td>
</tr>
<tr>
<td>CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling</td>
</tr>
<tr>
<td>CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected</td>
</tr>
<tr>
<td>CVE-2019-11135 (TSX Asynchronous Abort): Not affected</td>
</tr>
</tbody>
</table>

run-level 3 Aug 5 12:05
SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda4 btrfs 445G 19G 425G 5% /home

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSB-B200-M6
Serial: FCH24097576

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200, configured at 2666

BIOS:
BIOS Vendor: Cisco Systems, Inc.
BIOS Version: B200M6.4.2.1c.10.0723211453
BIOS Date: 07/23/2021
BIOS Revision: 5.22

(End of data from sysinfo program)

Compiler Version Notes
==============================================================================
<table>
<thead>
<tr>
<th>C</th>
<th>619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)</th>
</tr>
</thead>
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<tr>
<td>Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)</td>
<td></td>
</tr>
<tr>
<td>64, Version 2021.1 Build 20201112_000000</td>
<td></td>
</tr>
<tr>
<td>Copyright (C) 1985-2020 Intel Corporation. All rights reserved.</td>
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Compiler Version Notes (Continued)

C++, C, Fortran | 607.cactuBSSN_s(base)

Intel(R) C++ Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Fortran | 603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Fortran, C | 621.wrf_s(base) 627.cam4_s(base) 628.pop2_s(base)

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
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Base Compiler Invocation

C benchmarks:
icc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

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Base Compiler Invocation (Continued)

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-m64 -std=c11 -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-mbranches-within-32B-boundaries

Fortran benchmarks:
-m64 -Wl,-z,muldefs -DSPEC_OPENMP -xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Benchmarks using both Fortran and C:
-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Benchmarks using Fortran, C, and C++:
-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs
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The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:


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Tested with SPEC CPU®2017 v1.1.8 on 2021-08-05 14:28:05-0400.
Report generated on 2021-09-01 14:22:50 by CPU2017 PDF formatter v6442.
Originally published on 2021-08-31.