Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 5317, 3.00GHz)

![SPEC CPU 2017 Floating Point Rate Result](https://www.spec.org/)

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Aug-2021  
**Hardware Availability:** Apr-2021  
**Software Availability:** Dec-2020

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
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<tr>
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<td>48</td>
</tr>
<tr>
<td>554.roms_r</td>
<td>48</td>
</tr>
</tbody>
</table>

**Hardware**

- **CPU Name:** Intel Xeon Gold 5317  
- **Max MHz:** 3600  
- **Nominal:** 3000  
- **Enabled:** 24 cores, 2 chips, 2 threads/core  
- **Orderable:** 1.2 Chips  
- **Cache L1:** 32 KB I + 48 KB D on chip per core  
- **L2:** 1.25 MB I+D on chip per core  
- **L3:** 18 MB I+D on chip per core  
- **Memory:** 1 TB (32 x 32 GB 2Rx4 PC4-3200V-R, running at 2933)  
- **Storage:** 1 x 960 GB M.2 SSD SATA  
- **Other:** None

**Software**

- **OS:** SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default  
- **Compiler:** C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux  
- **Parallel:** No  
- **Firmware:** Version 4.2.1c released Jul-2021  
- **File System:** xfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** Not Applicable  
- **Other:** jemalloc memory allocator V5.0.1  
- **Power Management:** BIOS and OS set to prefer performance at the cost of additional power usage
SPEC CPU®2017 Floating Point Rate Result

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SPECrate®2017_fp_base = 217
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<td>769</td>
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<td>771</td>
<td>98.9</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC_CONF = "retain:true"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:

(Continued on next page)
# SPEC CPU®2017 Floating Point Rate Result

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9019

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---

## General Notes (Continued)

```bash
sync; echo 3 > /proc/sys/vm/drop_caches
numactl --interleave=all runcpu <etc>
```

**NA:** The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

**Yes:** The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

**Yes:** The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.


## Platform Notes

**BIOS Settings:**
- Adjacent Cache Line Prefetcher set to Disabled
- DCU Streamer Prefetch set to Disabled
- Sub NUMA Clustering set to Enabled
- LLC Dead Line set to Disabled
- Memory Refresh Rate set to 1x Refresh
- ADDDC Sparing set to Disabled
- Patrol Scrub set to Disabled
- Enhanced CPU performance set to Disabled
- Energy Efficient Turbo set to Enabled
- Processor C6 Report set to Enabled
- Processor C1E set to Enabled

**Sysinfo program**
/sysinfo

Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d

running on localhost Thu Aug  5 09:04:54 2021

**SUT (System Under Test) info as seen by some common utilities.**

For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

**From /proc/cpuinfo**
```
model name : Intel(R) Xeon(R) Gold 5317 CPU @ 3.00GHz
  2 "physical id"s (chips)
  48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 12
siblings : 24
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11
```

(Continued on next page)
## Platform Notes (Continued)

From `lscpu` from `util-linux 2.33.1`:
- Architecture: x86_64
- CPU op-mode(s): 32-bit, 64-bit
- Byte Order: Little Endian
- Address sizes: 46 bits physical, 57 bits virtual
- CPU(s): 48
- On-line CPU(s) list: 0-47
- Thread(s) per core: 2
- Core(s) per socket: 12
- Socket(s): 2
- NUMA node(s): 4
- Vendor ID: GenuineIntel
- CPU family: 6
- Model: 106
- Model name: Intel(R) Xeon(R) Gold 5317 CPU @ 3.00GHz
- Stepping: 6
- CPU MHz: 2833.251
- CPU max MHz: 3600.0000
- CPU min MHz: 800.0000
- BogoMIPS: 6000.00
- Virtualization: VT-x
- L1d cache: 48K
- L1i cache: 32K
- L2 cache: 1280K
- L3 cache: 18432K
- NUMA node0 CPU(s): 0-5, 24-29
- NUMA node1 CPU(s): 6-11, 30-35
- NUMA node2 CPU(s): 12-17, 36-41
- NUMA node3 CPU(s): 18-23, 42-47
- Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtdr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invvpicid_single ssbd mba ibrs ibrs_enabled tpr_shadow vmi flexpriority ept vpid ept_ad fsproj base tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni avx512bw avx512vl xsaveopt xsaves xsavec xgetbv1 xsaves cqm_llc cqm_occnp_llc cqm_mbm_total cqm_mbb_local wbnoinvd dtc ht ia32e ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req avx512vbm1 umip pku ospke avx512_vbm2 gfni vaes vpclmulqdq avx512_vnni avx512_bitalg tme avx512_vpopcntd q1a57 rdpid md_clear pconfi flush lld arch_capabilities

/proc/cpuinfo cache data
- cache size: 18432 KB

(Continued on next page)
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Platform Notes (Continued)

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 24 25 26 27 28 29
node 0 size: 257563 MB
node 0 free: 257321 MB
node 1 cpus: 6 7 8 9 10 11 30 31 32 33 34 35
node 1 size: 258044 MB
node 1 free: 257791 MB
node 2 cpus: 12 13 14 15 16 17 36 37 38 39 40 41
node 2 size: 258011 MB
node 2 free: 257751 MB
node 3 cpus: 18 19 20 21 22 23 42 43 44 45 46 47
node 3 size: 257764 MB
node 3 free: 257476 MB
node distances:
node   0   1   2   3
0: 10 11 20 20
1: 11 10 20 20
2: 20 20 10 11
3: 20 20 11 10

From /proc/meminfo
MemTotal: 1056137060 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
os-release:
  NAME="SLES"
  VERSION="15-SP2"
  VERSION_ID="15.2"
  PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
  ID="sles"
  ID_LIKE="suse"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

(Continued on next page)
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Platform Notes (Continued)

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2018-3639 (Speculative Store Bypass): Mitigation: usercopy/swaps barriers and __user pointer sanitization
CVE-2017-5753 (Spectre variant 1): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2017-5715 (Spectre variant 2):
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Aug 5 09:03

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda6 xfs 812G 13G 799G 2% /home

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSB-B200-M6
Serial: FCH2409757J

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
32x 0xCE00 M393A4K40DB3-CWE 32 GB 2 rank 3200, configured at 2933

BIOS:
BIOS Vendor: Cisco Systems, Inc.
BIOS Version: B200M6.4.2.1c.10.0723211453
BIOS Date: 07/23/2021
BIOS Revision: 5.22

(End of data from sysinfo program)

Compiler Version Notes

********************************************************************************
C | 519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)
********************************************************************************
(Continued on next page)
## Compiler Version Notes (Continued)

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Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

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Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
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Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
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Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icx

Benchmarks using both C and C++:
icpx icx

Benchmarks using Fortran, C, and C++:
icpx icx ifort

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.ibm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64

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**Base Optimization Flags (Continued)**

Benchmarks using Fortran, C, and C++ (continued):
- -qopt-multiple-gather-scatter-by-shuffles
- -mbranches-within-32B-boundaries -nostandard-realloc-lhs
- -align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.8 on 2021-08-05 12:04:53-0400.
Report generated on 2021-09-01 14:23:10 by CPU2017 PDF formatter v6442.
Originally published on 2021-08-31.